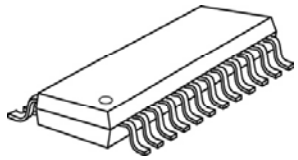
16-Channel PWM Constant Current LED Driver for 1:32 Time-Multiplexing Applications

Features

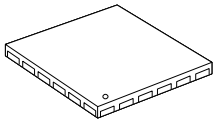
- 3V-5.5V supply voltage
- 16 constant current output channels
- Constant output current range:
  - 0.5~20mA @ 5V supply voltage
  - 0.5~10mA @ 3.3V supply voltage
- Excellent output current accuracy:
  Between channels:：<±2.5%(Max.)
  Between ICs: <±3%(Max.)
- Built-in 16K-bit SRAM to support time-multiplexing for 1 ~ 32 scans
- 14-bit /13-bit color depth PWM control to improve visual refresh rate
- 6bit current gain，12.5%~200%
- LED failure isolation
  -LED failure induced cross elimination
- LED open detection
- Integrating ghost elimination circuit
- GCLK multiplier technology
- Maximum DCLK frequency: 30MHz

Shrink SOP



GP: SSOP24L-150-0.64

Quad Flat No-leads



GFN: QFN24L-4x4-0.5

Product Description

MBI5153 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 14-bit / 13-bit color depth. MBI5153 features a 16-bit shift register which converts serial input data into each pixel's gray scale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:32 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5153 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

MBI5153 drives the corresponding LEDs to the brightness specified by image data. With MBI5153, all output channels can be built with 14-bit color depth (16,384 gray scales). When building a 14-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity.

Through compulsory error detection, MBI5153 detects individual LED for open-circuit errors without extra components. MBI5153 equipped an innovative cross elimination function, and it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination circuit eases the ghost problems.

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Block Diagram

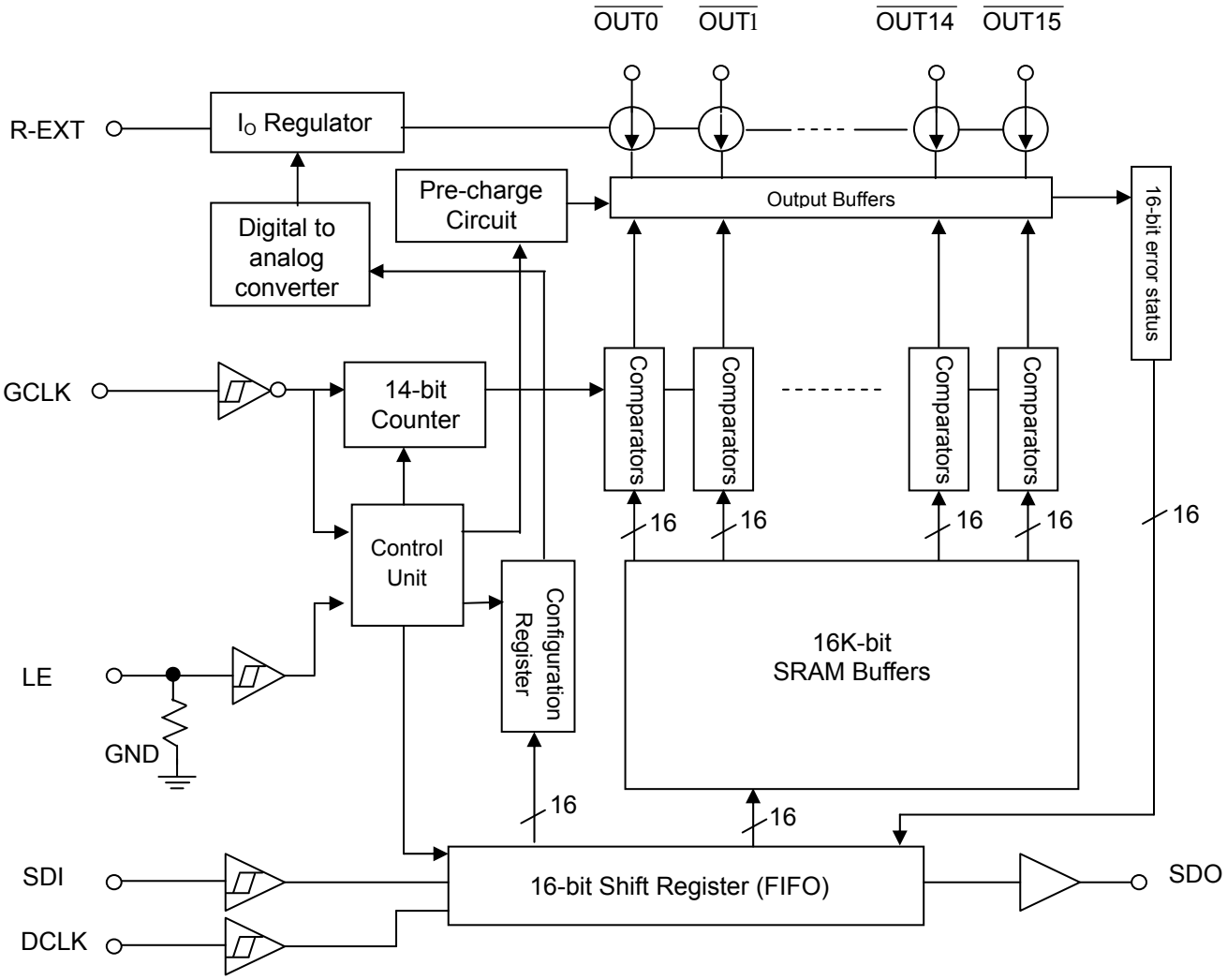
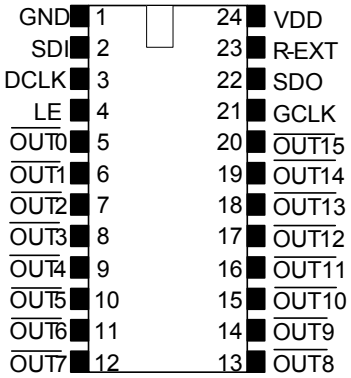
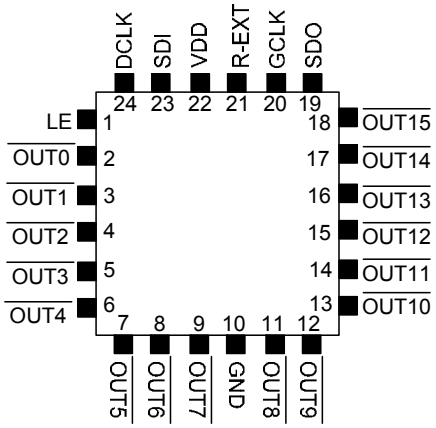


Figure 1

Pin Configuration



MBI5153 GP



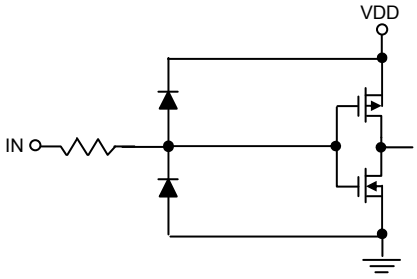
GFN

Terminal Description

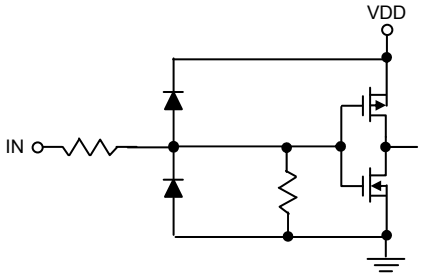
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock compared with input data.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

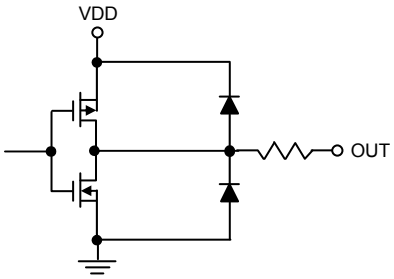
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Input Pin Voltage (SDI, DCLK, GCLK, LE)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Port		V_{DS}	-0.5~17	V
Output Current		I_{OUT}	+22	mA
GND Terminal Current		I_{GND}	360	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP Type	P_D	1.79	W
	GFN Type		3.12	
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GP Type	$R_{th(j-a)}$	69.5	°C/W
	GFN Type		40.01	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	HBM	Class 3B (8000V)	-
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	MM	Class C (≧400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	-		-	0.5	-	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK=0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	4.5	5.5	mA
		I_{DD}(off) 3	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	5	6	
		I_{DD}(off) 4	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	6.5	8	
	"On" (SDI= DCLK=5MHz, GCLK=20MHz)	I_{DD}(on) 9	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =On		-	6.5	8	
		I_{DD}(on) 10	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =On		-	8.5	10	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	10	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	-		-	0.3	-	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK=0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	4.5	5	mA
		I_{DD}(off) 2	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	4.5	5.5	
		I_{DD}(off) 3	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	6.0	7.0	
	"On" (SDI= DCLK=5MHz, GCLK=20MHz)	I_{DD}(on) 2	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	6.0	7.0	
		I_{DD}(on) 3	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	7.5	9.0	

*One channel on.

Test Circuit for Electrical Characteristics

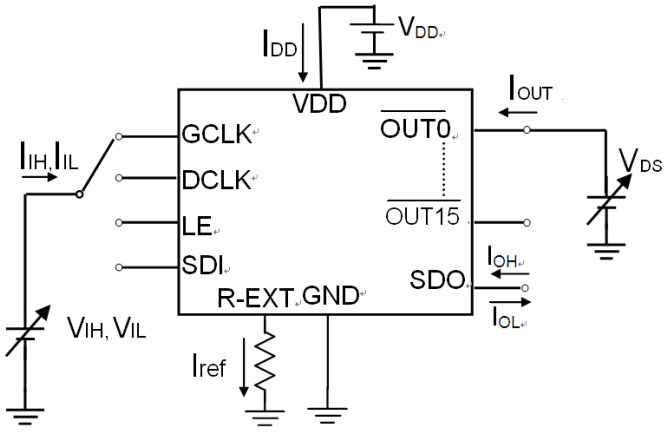


Figure 2

Switching Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	5	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		8	-	-	ns
	LE ↓ (Vsync) – GCLK	t_{SU2}		1200			ns
	LE ↓ – DCLK ↑	t_{SU3}		50			ns
Hold Time	DCLK ↑ - SDI	t_{H0}		6	-	-	ns
	DCLK ↑ - LE	t_{H1}		8	-	-	ns
	GCLK – LE ↑ (Vsync)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	22	25	ns
	GCLK – $\overline{OUT2n}$ *	t_{PD1}		-	35	-	ns
	LE – SDO	t_{PD2}***		-	30	40	ns
Staggered Delay of Output	$\overline{OUT2n+1}$ **	t_{DL1}		-	5	-	ns
Pulse Width	LE	$t_{w(LE)}$		15			ns
Command to Command		Tcc		50	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency***		F_{GCLK}		-	-	33	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}				16.6	MHz
Min Clock(GCLK/DCLK) Pulse Width****		$t_{W(CLK)}$		12	-	-	ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory Error Detection Operation time*****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	15	25	ns
Output Fall Time of Output Ports		t_{OF}		-	15	25	ns
Dead Time		t_{dth}		300			ns
Dead Time (Low state)		t_{dtl}		1200	-	-	ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE – DCLK ↑	t_{SU1}		10	-	-	ns
	LE ↓ (Vsync) – GCLK	t_{SU2}		1200	-	-	ns
	LE ↓ – DCLK ↑	t_{SU3}		52			ns
Hold Time	DCLK ↑ - SDI	t_{H0}		8	-	-	ns
	DCLK ↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE ↓ (Vsync)	t_{H2}		300	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25	30	ns
	GCLK –$\overline{OUT2n}$*	t_{PD1}		-	45	-	ns
	LE – SDO	t_{PD2}***			40	50	ns
Staggered Delay of Output	$\overline{OUT2n+1}$ **	t_{DL1}		-	8	-	ns
Pulse Width	LE	$t_{w(LE)}$		16			ns
Command to Command		tcc		52	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	20	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}				10	MHz
Min Clock(GCLK/DCLK) Pulse Width****		$t_{W(CLK)}$		13			ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20		-	%
Compulsory Error Detection Operation time*****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}			25	35	ns
Output Fall Time of Output Ports		t_{OF}			25	35	ns
Dead Time		tdth		300	-	-	ns
Dead Time (Low state)		tdtl		1200	-	-	ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Test Circuit for Switching Characteristics

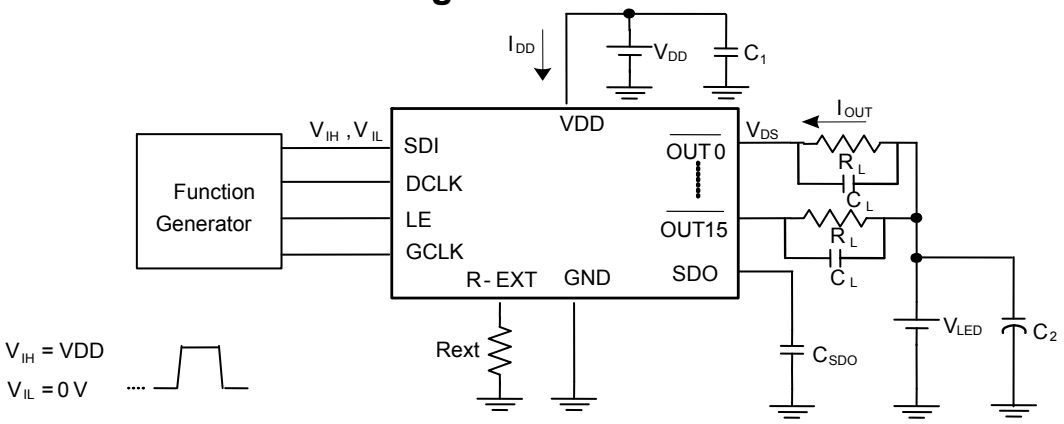
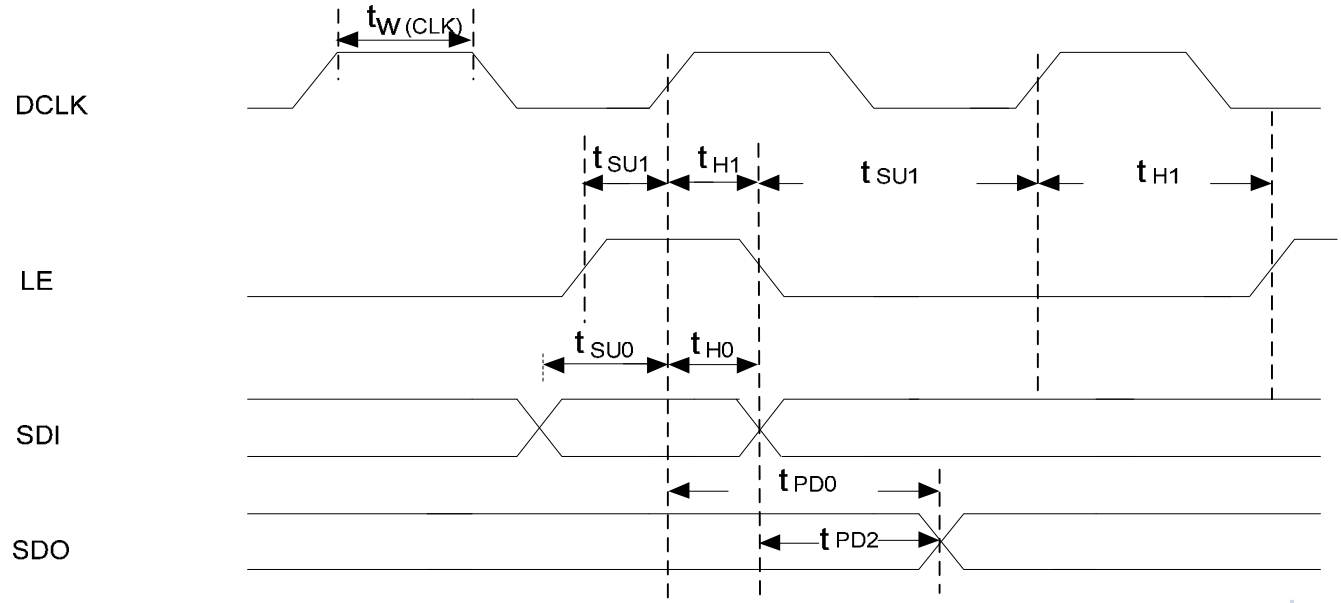
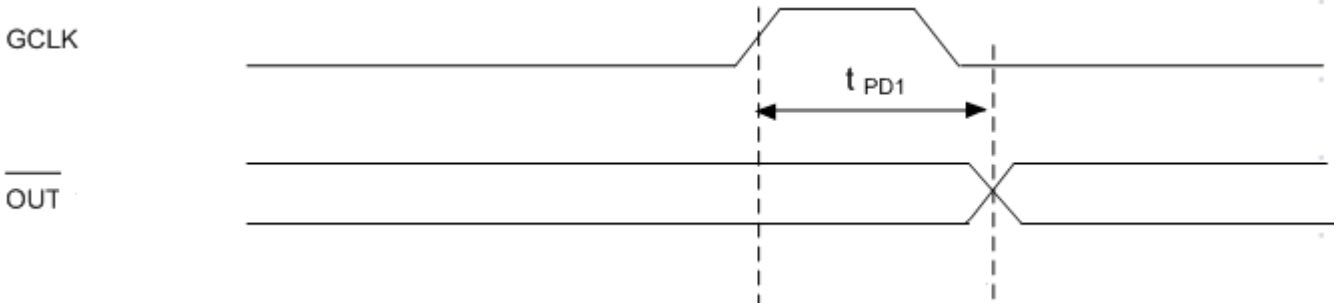
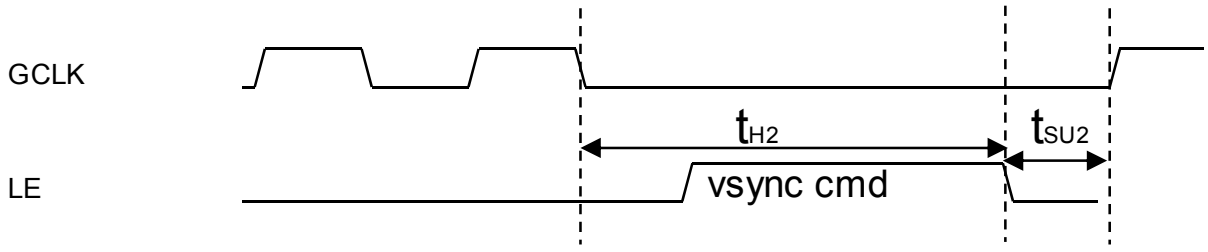


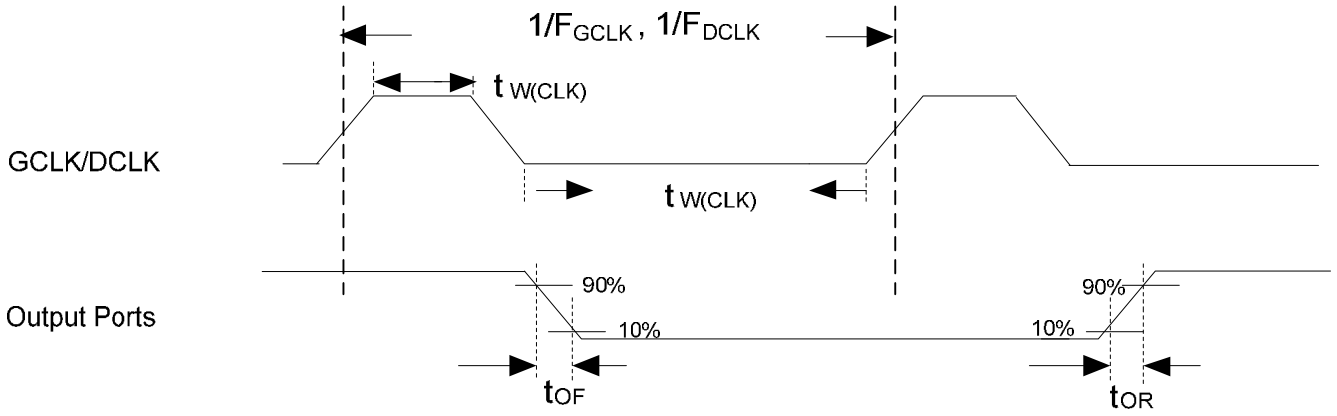
Figure 3

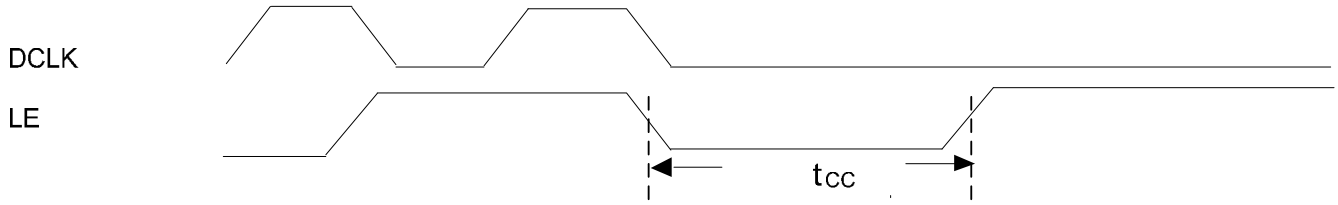
Timing Waveform

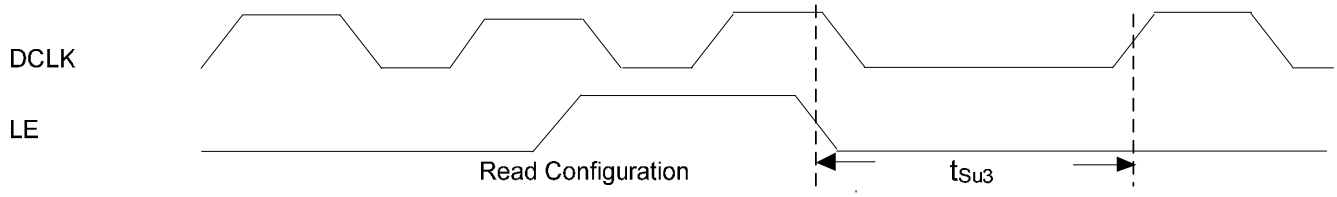


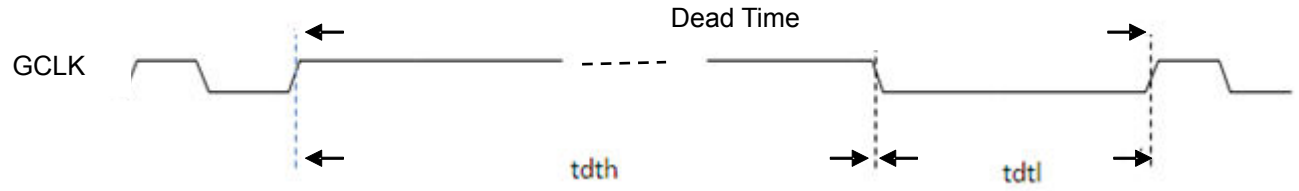





1/FGCLK , 1/FDCLK
tW(CLK)
GCLK/DCLK
tW(CLK)
Output Ports
90%
10%
90%
10%
tOF
tOR


DCLK
LE
tCC


DCLK
LE
Read Configuration
tSu3


Dead Time
GCLK
tdth
tdtl

Control Command

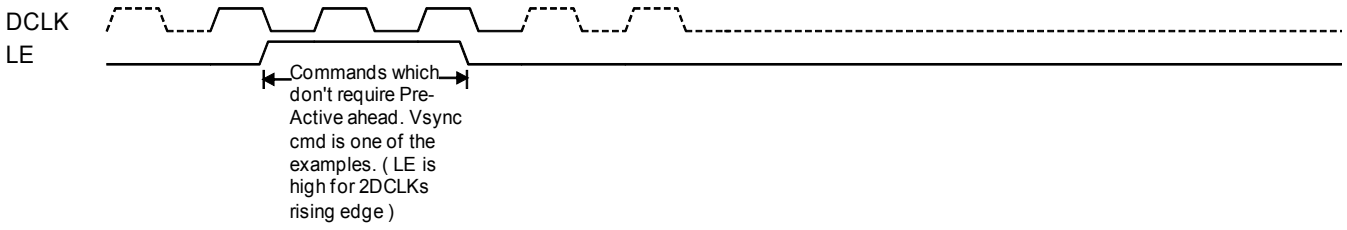
Command Name	Signals Combination		Description
	LE	Number of DCLK Rising Edge when LE is asserted	Action of Command
Stop Compulsory Error detection	High	1	Stop compulsory LED open detection.
Data Latch	High	1	Serial data are transferred to the input data buffers.
VSYNC	High	2	Vertical Synchronal signal. Displaying frame will be updated to output channel.
Write Configuration 1*	High	4	Serial data are written to the configuration register.1
Read Configuration 1	High	5	Serial data are read from the configuration register.1
Start Compulsory Error detection	High	7	Start compulsory LED open detection
Write Configuration 2*	High	8	Serial data are written to the configuration register.2
Read Configuration 2	High	9	Serial data are read from the configuration register.2
Software Reset	High	10	Reset the behavior of MBI5153 except the value of configuration registers.
Pre-Active	High	14	Pre-Active command needs to be sent before “Write Configuration” command.

*Those commands can only be activated after Pre-Active command; otherwise, they will be invalid.

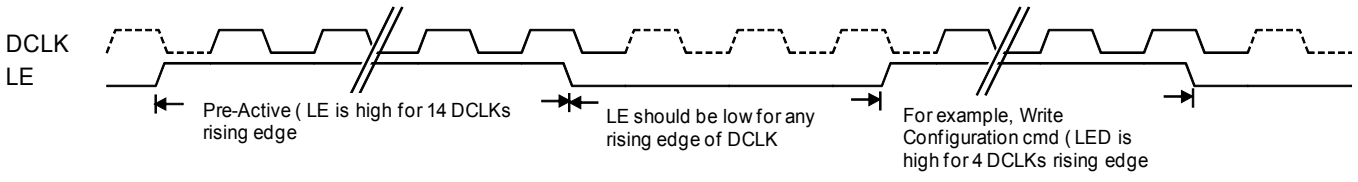
Note: When the power is on, Vsync command will be valid only after 16 times of “Data Latch” commands that have been sent in advance.

The following figures show the waveforms of commands which require or don’t require “Pre-Active” ahead.

Commands which don't require Pre-Active ahead



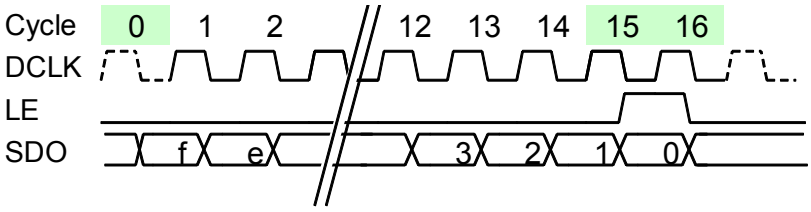
Commands which require Pre-Active ahead



Waveform of Commands

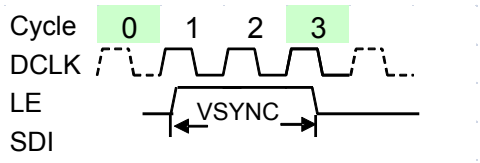
The following figures show the waveforms of each command.

Data Latch



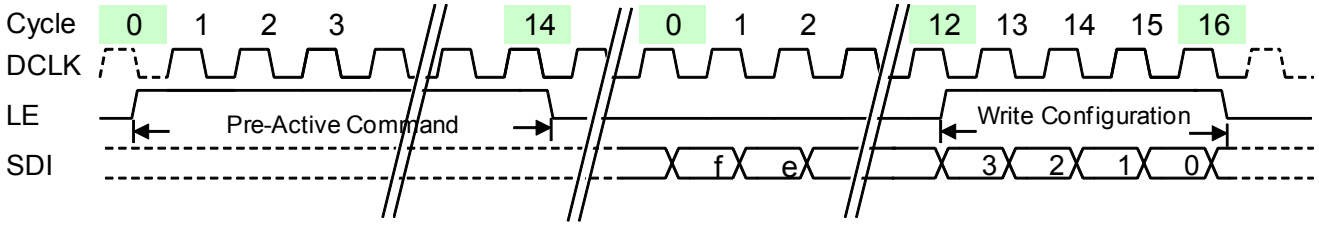
Data Latch command is used to latch the 16-bit shift register from SDI to internal SRAM buffer. When this command is received, the last 16 bits data before the falling edge of LE will be latched into SRAM, as shown in the above waveform, and MSB bit needs to be sent first.

Vertical Sync (VSYNC)



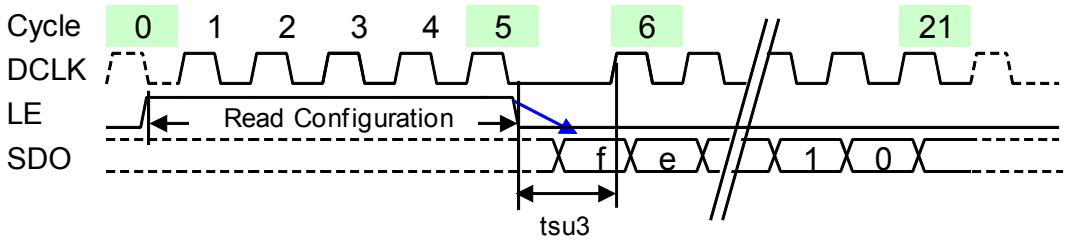
"VSYNC" command is used to update frame data on output channels ($\overline{OUT0}$~ $\overline{OUT15}$). There are some timing limitations between signal "LE" and "GCLK"; and please refer to the section of "Vsync Command Operation" for details.

Write Configuration



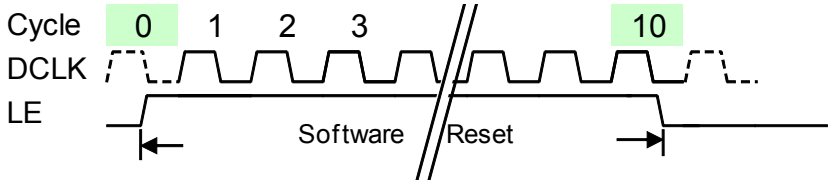
"Write configuration" command is used to program the configuration register of MBI5153. The "Pre-Active" command must be sent in advance. When this command is received, the last 16 bits data before the falling edge of LE will be latched into configuration register, as shown in the above waveform, and MSB bit needs to be sent first.

Read Configuration



"Read configuration" command is used to read the configuration register of MBI5153. When this command is received, the 16-bit data of configuration register will be shifted out from SDO pin, as shown in the above waveform, and MSB bit will be shifted out first.

Software Reset



"Software reset" command makes MBI5153 go back to the initial state except configuration register value. After this command is received, the output channels will be turned off and will display again with last gray-scale value after new "Vsync" command is received.

Definition of Configuration Register 1

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	101011					

Default setting of configuration register is 16'h032B

Bit	Attribute	Definition	Value	Function
F	Read/Write	Lower ghost elimination	0 (Default)	0:Disable
				1:Enabled
E~D	Reserved	Reserved	00 (Default)	Reserved
B-8	Read/Write	Number of scan lines	00000 00001 00010 00011 (**Default**) ~ 11111	00000: 1 line 00001: 2 lines 00010: 3 lines 00011: 4 lines …….. 11110: 31 lines 11111: 32 lines
7	Read/Write	Gray scale mode	0 (Default)	The 16384 GCLKs (14-bit) PWM cycle is divided into 32 sections, and each section has 512 GCLKs.
			1	The 8192 GCLKs(13-bit) PWM cycle is divided into 16 sections, and each section has 512 GCLKs.,
6	Read/Write	GCLK multiplier	0 (Default)	GCLK multiplier disable
			1	GCLK multiplier enable
5~0	Read/Write	Current gain adjustment	000000~111111	6'b101011 (Default) Allow 64-step programmable current gain from 12.5 % to 200%

Definition of Configuration Register 2

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Default setting of configuration register is 16'h032B

Bit	Attribute	Definition	Value	Function
F~B	Reserved	Reserved	Reserved	Reserved
A	Read/Write	Double refresh rate	0(Default)	0: Disable 1: Enable
9~4	Reserved	Reserved	Reserved	Reserved
3~1	Read/Write	dim line compensation	000 (Default)	000: 0 ns, 100: 20ns 001: 5 ns, 101: 25ns 010: 10 ns, 110: 30ns 011: 15 ns, 111: 35ns
0	Reserved	Reserved	Reserved	Reserved

Number of Scan Line

MBI5153 supports 1 to 32 scan lines. Please set the configuration register1 bit [C:8] according to the application. The default value '00011' is 4 scan lines.

Gray Scale Mode and Scan-type S-PWM

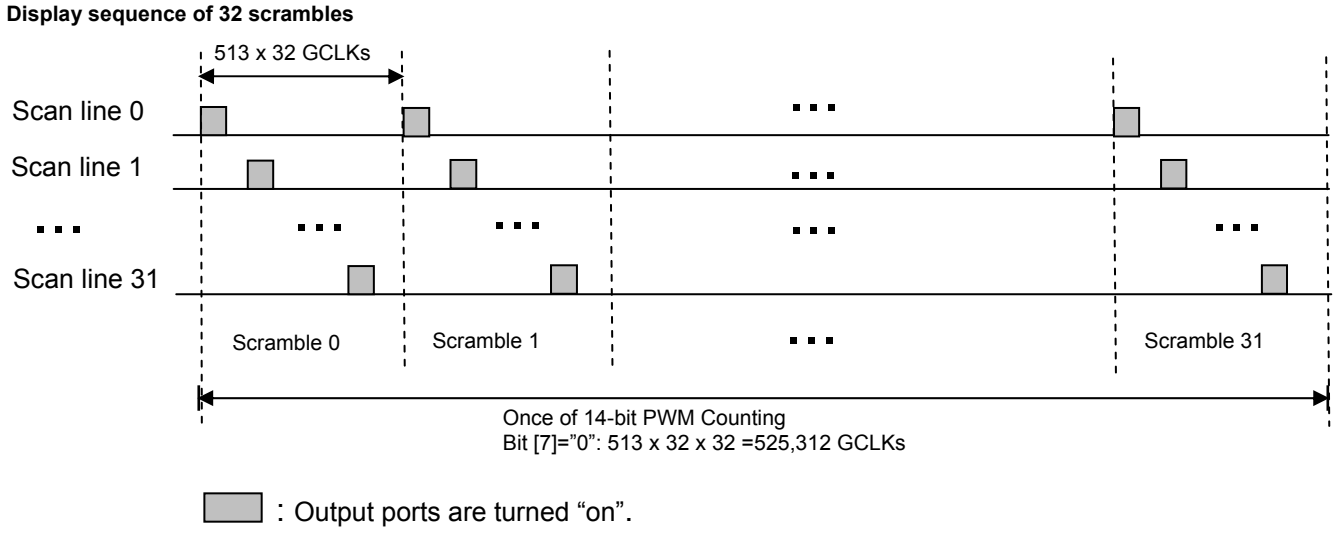
MBI5153 provides a selectable 14-bit or 13-bit gray scale by setting the configuration register1 bit [7]. The default value is set to '0' for 14-bit color depth. In 14-bit gray scale mode, users should still send 16-bit data with 2-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

MBI5153 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be broken into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

GCLK multiplier

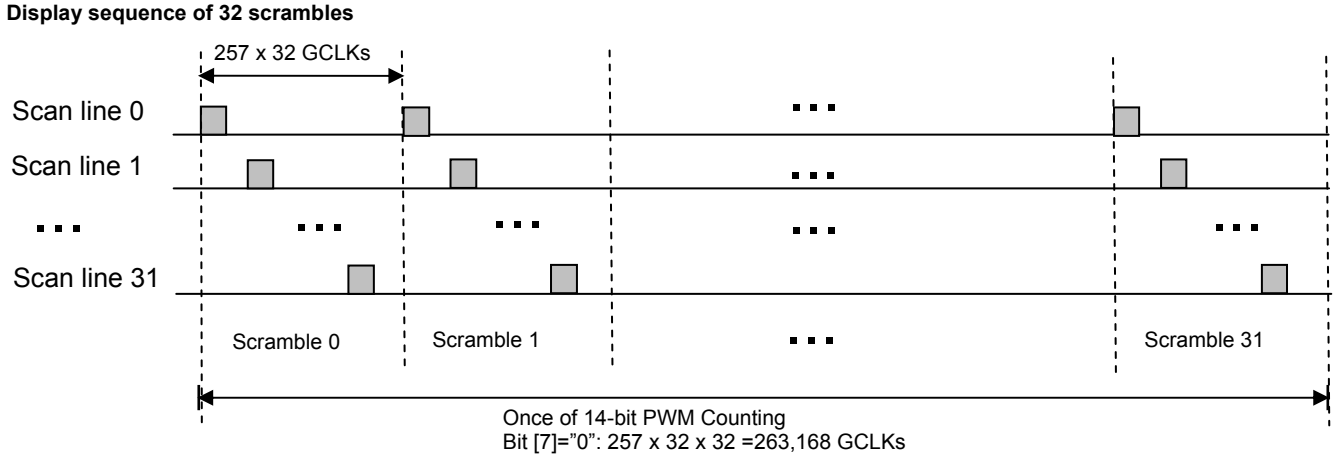
MBI5153 provides a GCLK multiplier function by setting the configuration register1 bit [6]. The default value is set to '0' for GCLK multiplier disable.

GCLK multiplier disabled (configuration register1 bit [6] = 0)



: Output ports are turned "on".

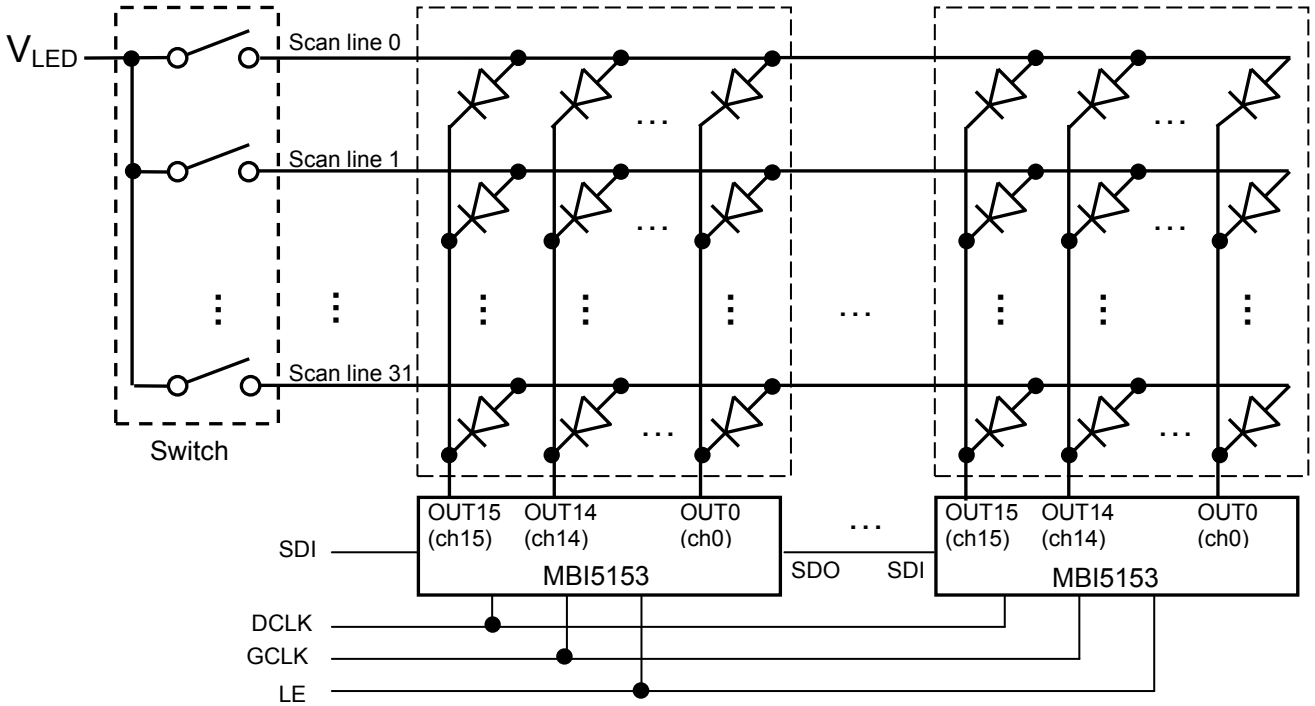
GCLK multiplier enabled (configuration register1 bit [6] = 1)



: Output ports are turned "on".

Operation Principal

Scan type application structure



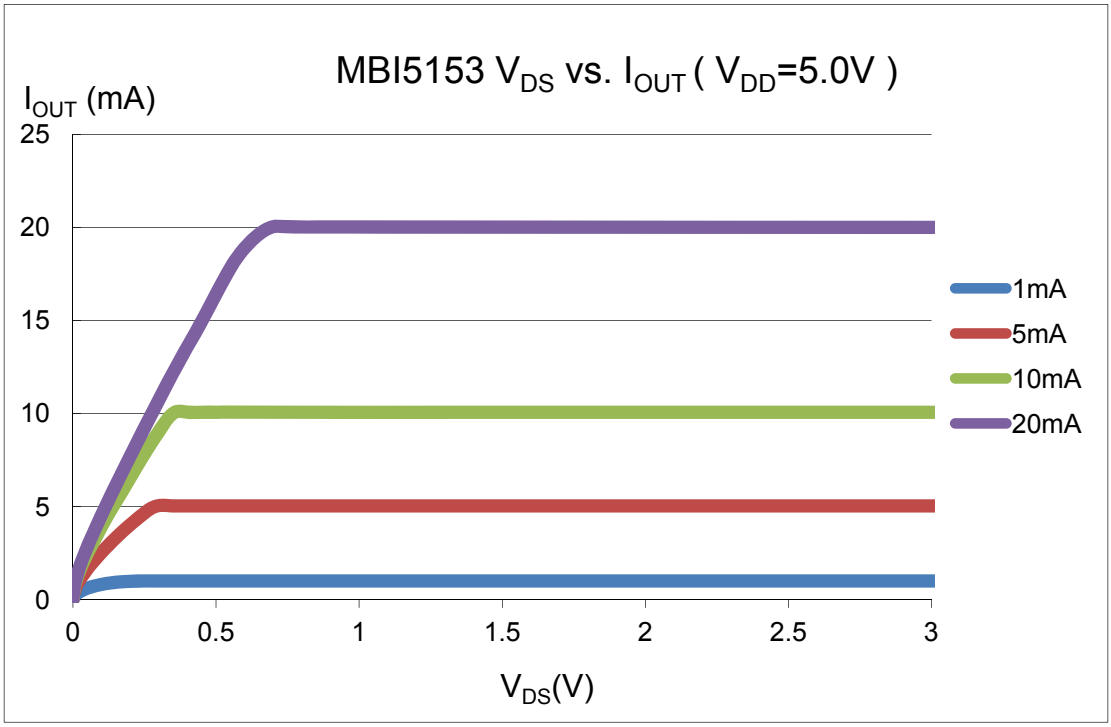
The above figure shows the suggested application structure of scan type scheme with 32 scan lines. The gray-scale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 16 channels ($\overline{OUT0}$ ~ $\overline{OUT15}$) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage will be described in the application note.

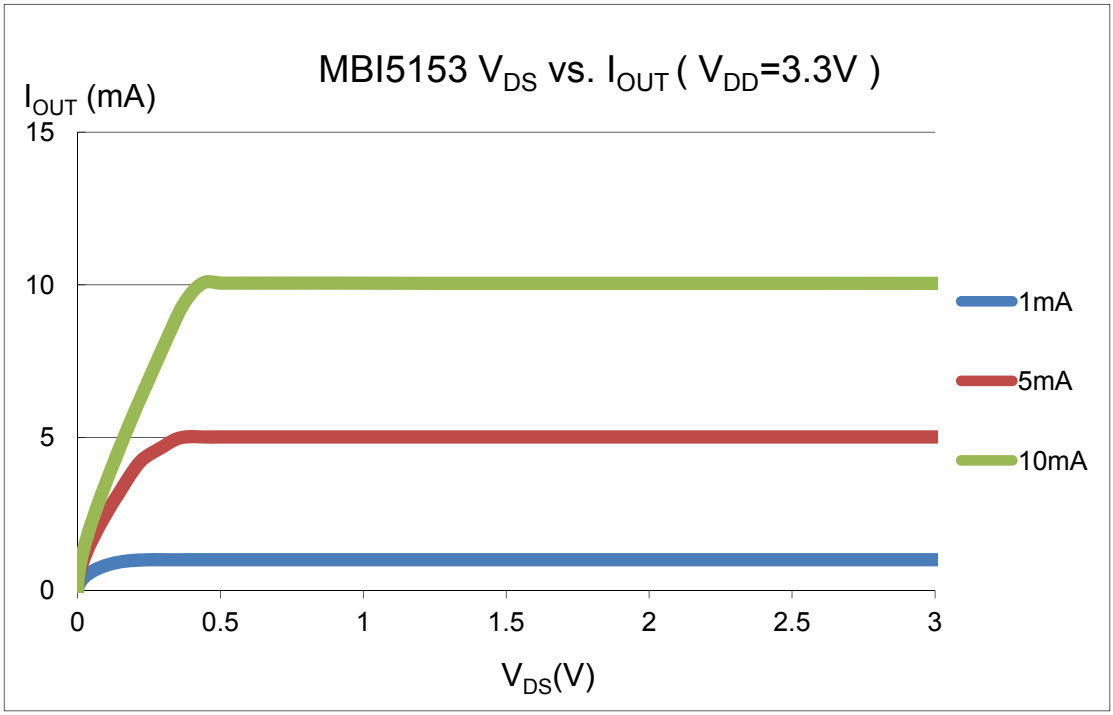
Constant Current

In LED display application, MBI5153 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximuml current variation between channels is less than 2.5%, and that between ICs is less than ±3%

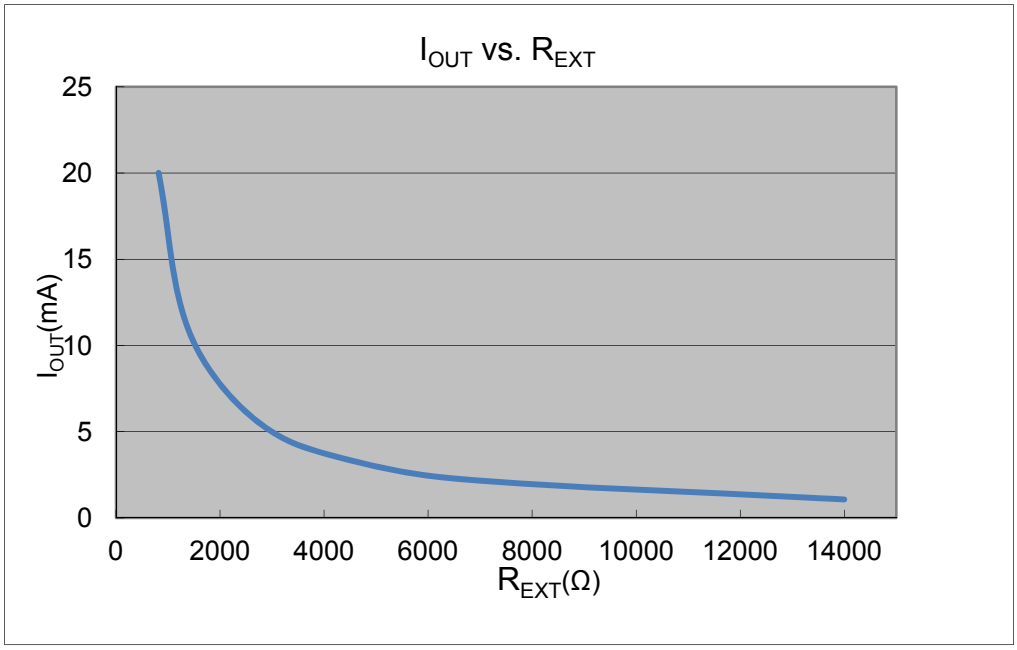
2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

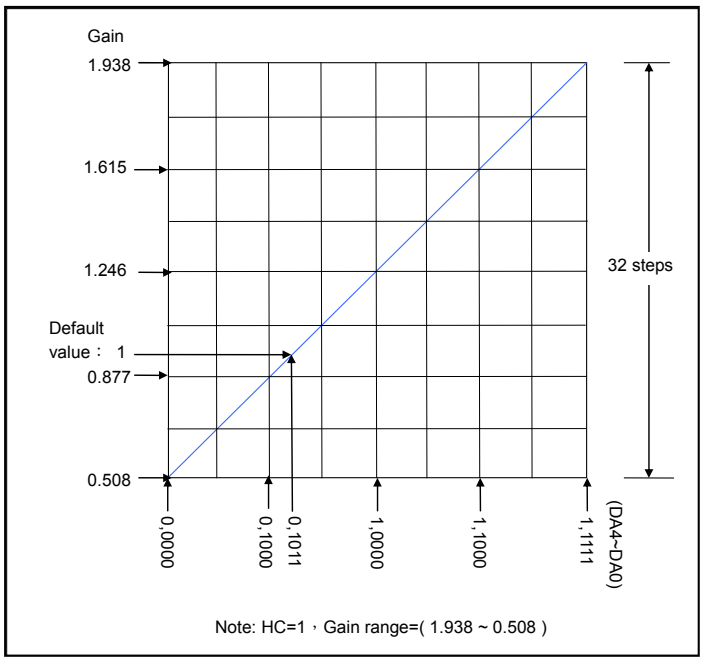


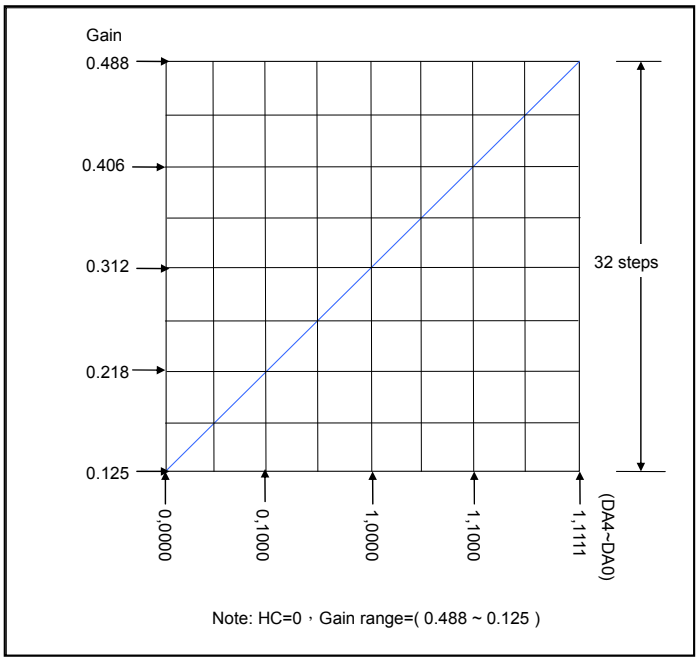
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.61Volt x G; I_{OUT}= ($V_{R\text{-}EXT}/R_{ext}$) x24.0

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit5 – bit0 of the configuration register. The default value of G is 1. The formula and setting for G are described in next section.

Current Gain Adjustment





The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number, i.e., ranging from 6'b000000 to 6'b111111, these bits allow user to set the output current gain up to 64 levels. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0

1. Bit 5 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 4 to bit 0 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

Package Power Dissipation (PD)

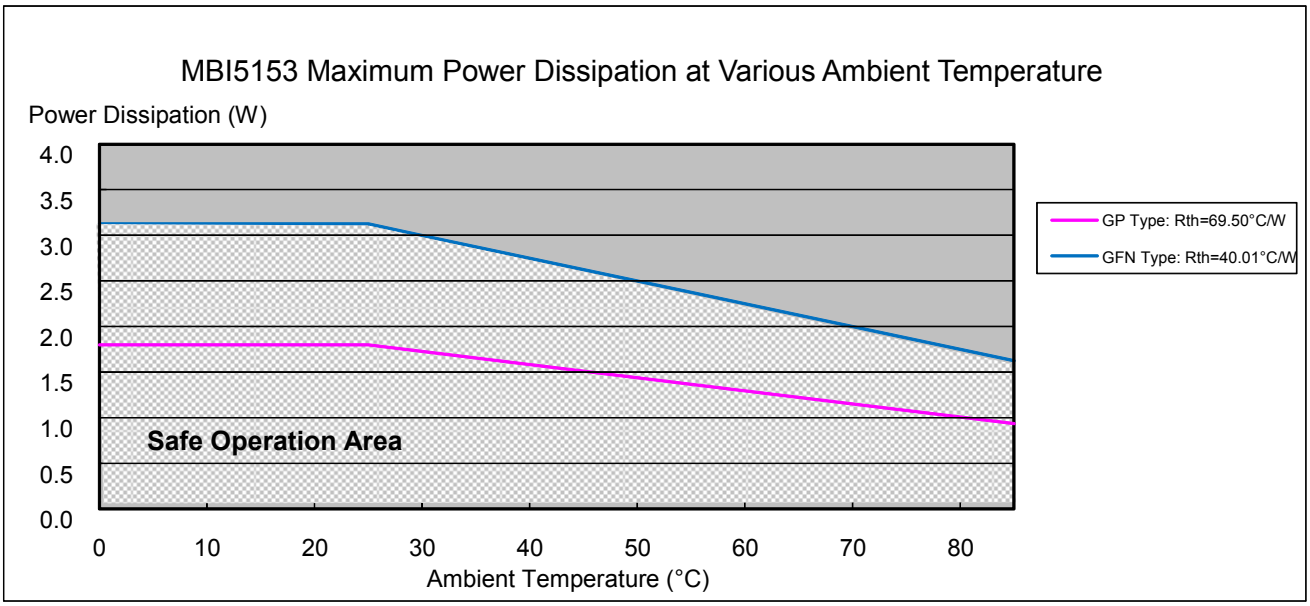
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	69.50	1.79
GFN	40.01	3.12

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



LED Supply Voltage (V_{LED})

MBI5153 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=1~20mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

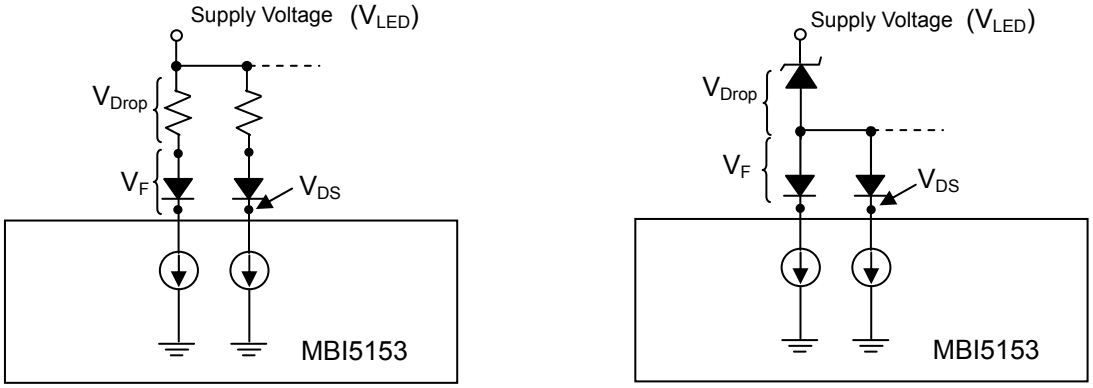


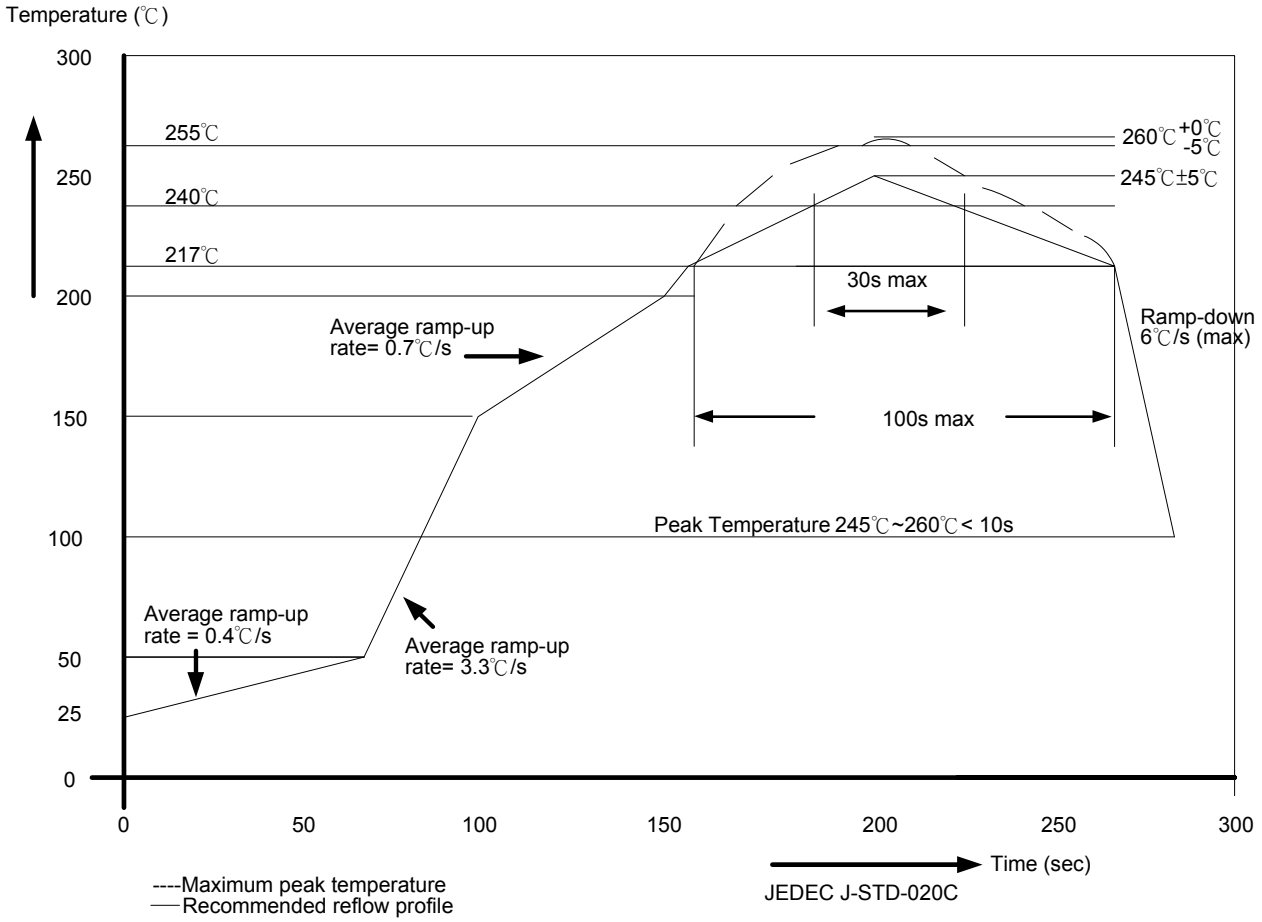
Figure 5

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

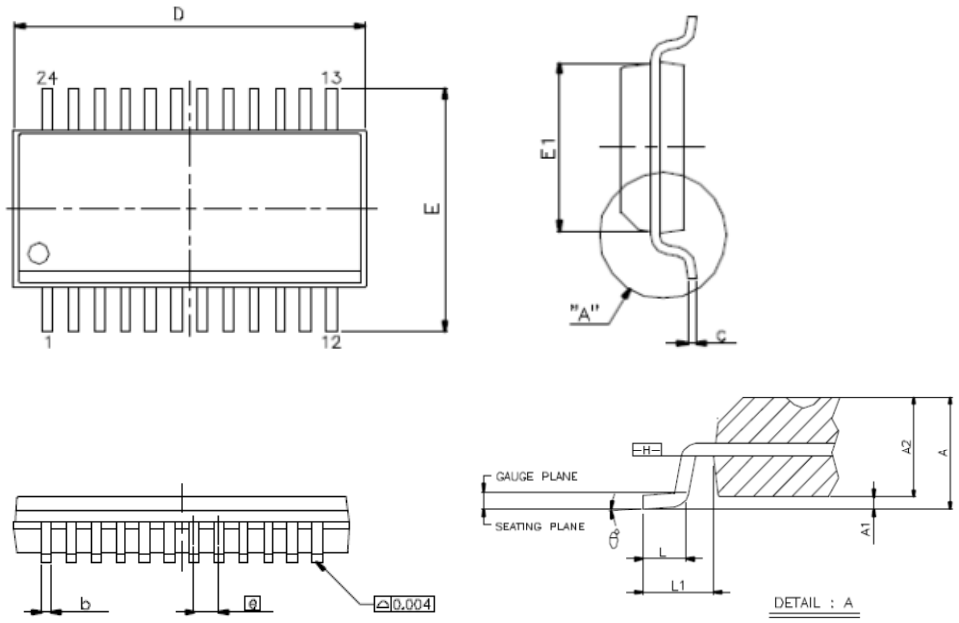
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

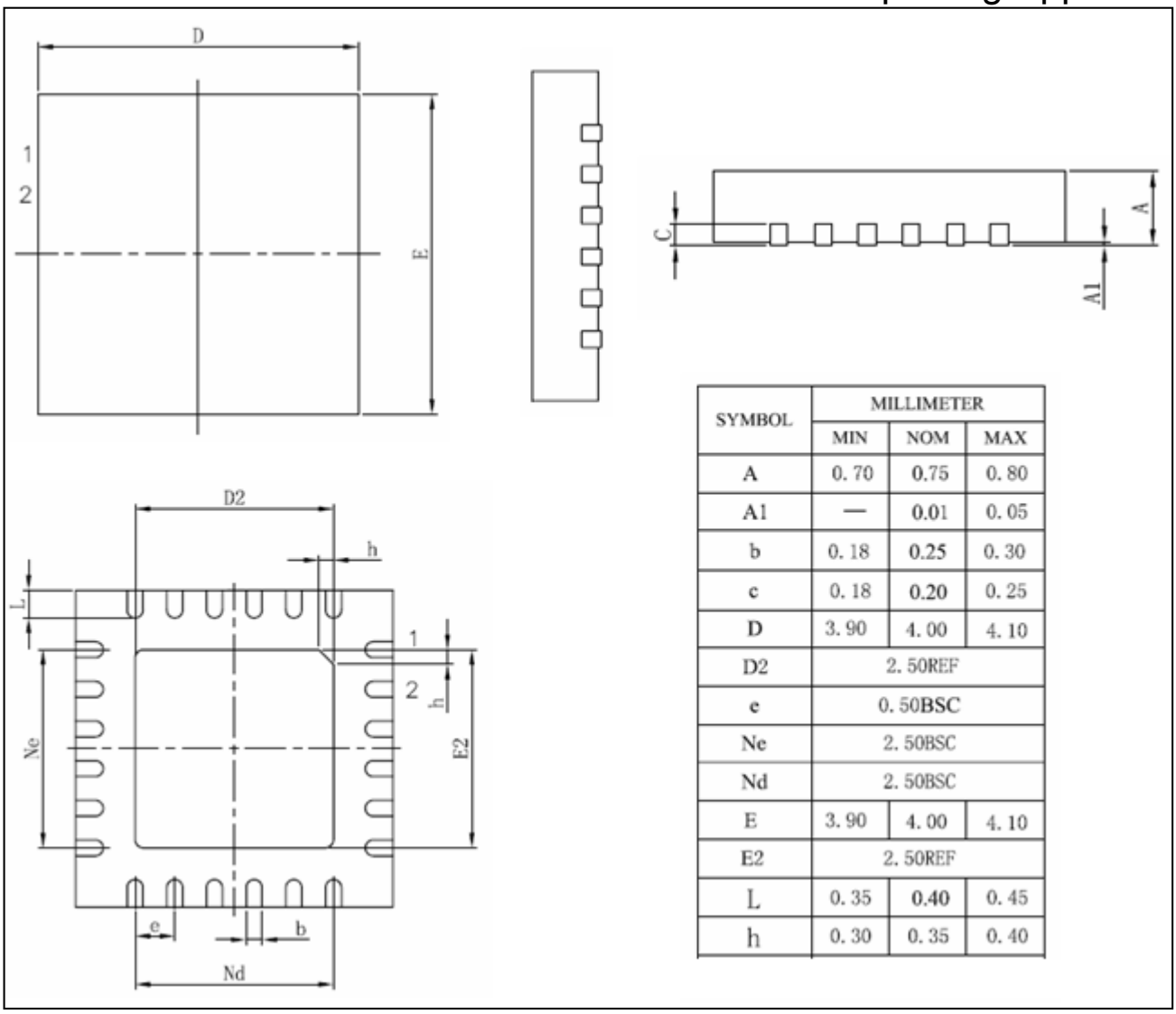
*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

MBI5153 GP Outline Drawing

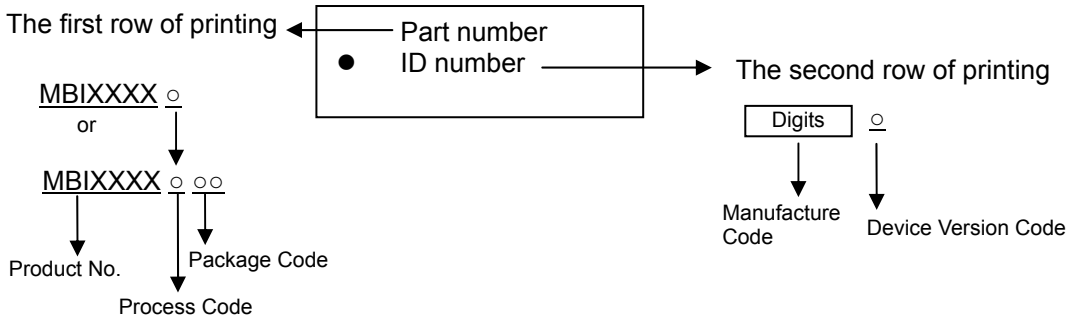


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MBI5153GFN Outline Drawing

Note: The unit of the outline drawing is millimeter (mm).

Product Top Mark Information



Product Revision History

Datasheet Version	Devise Version Code
V1.00	A

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5153GP-A	SSOP24L-150-0.64	0.11
MBI5153GFN-A	QFN24L-4*4-0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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MBI5051/MBI5052/MBI5053 Application Note

Forward

MBI5051/52/53 uses the embedded Pulse Width Modulation (PWM) to control LED current. In contrast to the traditional LED driver uses an external PWM signal to achieve the PWM function, MBI5051/52/53 has more outstanding behavior in gray scale performance and is suitable for LED full-color display.

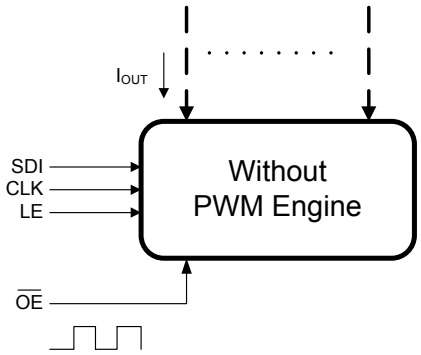

Figure 1. The traditional LED driver

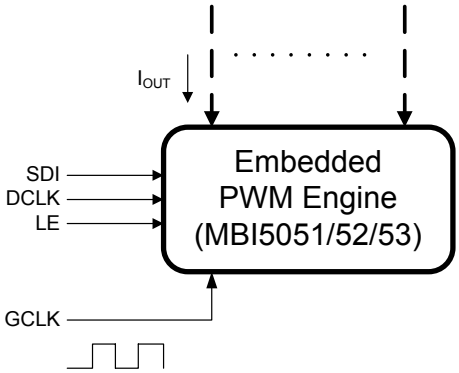

Figure 2. PWM-Embedded LED driver

Figure 1 shows the scheme of the traditional LED driver. It controls the LED current (I_{OUT}) and brightness by PWM signal through $\overline{OE}$ pin. The signal of $\overline{OE}$ will suffer distortion and decay in long distance transmission, and furthermore causing poor LED brightness control while using more gray scale bits. Figure 2 is the scheme of PWM-Embedded LED driver, the Gray Scale Clock (GCLK) is used to trigger the internal PWM counter and output a PWM pulse to control the LED current. Even in the applications of long distance transmission and high gray scale bits, the distorted and decayed GCLK will not affect the LED brightness control. Since GCLK is the trigger of PWM counter, the variable pulse width won't affect the internal PWM.

Moreover, the traditional PWM-Embedded LED driver requires a very fast DCLK frequency to input new data when the scan line changed. However, by MBI5051/52/53, the whole frame data can be inputted due to the embedded 4/8/16 bit SRAM, therefore the DCLK frequency can be slower. Compare to the traditional PWM driver, the MBI5051/52/53 can achieve higher gray scale in time multiplexing application.

This article provides the application information of MBI5051/52/53, such as the input method of image data and the setting of gray scale data. The detail operations are described in the following section.

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Section 1: Principle of Operations

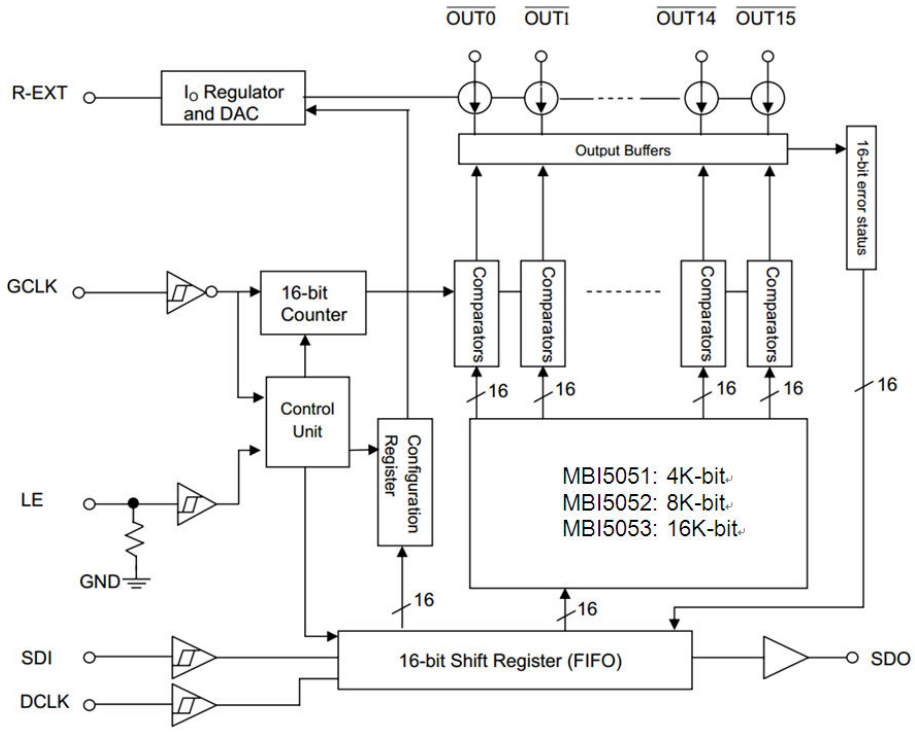

Figure 3. Internal block diagram of MBI5051/52/53

Figure 3 shows the internal block diagram of MBI5051/52/53, the function of each pin is described below.

Input Pins of Control Signals

DCLK: Data Clock Input pin

SDI: Gray Scale Data Input pin

LE: The combination of LE and DCLK can be used to control command.

The gray scale data of MBI5051/52/53 is the combination of DCLK, SDI and LE. On the rising edge of DCLK, MBI5051/52/53 reads one bit data from SDI pin and inputs to the internal 16-bit shift register. The LE pin handles the “data latch” command of the internal 16-bit shift register.

Control Signals Output Pin

SDO: Serial Data Output pin. The SDO of first device is connected to the SDI pin of second device and so on. The gray scale data can be sent to next IC.

PWM Counter Clock Input Pin

GCLK: PWM Counter Input pin. The frequency of GCLK determines the count speed of the internal PWM counter, and also the output frequency of $\overline{OUT0}$~$\overline{OUT15}$.

Current Setting Pin

R-EXT: This pin is used to connect an external resistor to set up the output current for all output channels.

LED Driver Output Pin

$\overline{OUT0}$~$\overline{OUT15}$: Output Channel pins. Connects to the LED and controls the LED current.

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Section 2: The Basic Settings of Gray Scale

In the time multiplexing application, the sequence of input data starts from scan line 1, scan line 2, until scan line M (M≦8/16/32). MBI5051/52/53's 16 channels can perform different gray scale data individually, so the data length of 16 channels must be 256 bits (16 bits x 16 channels =256 bits).

Example 1

Number of IC: 1

Number of scan line: 32

Depth of PWM control: 16- bit

As shown in figure 4, the data of ch15 need to be sent first, and then follow the sequence of ch14to ch0, and then LE executes the data latch.

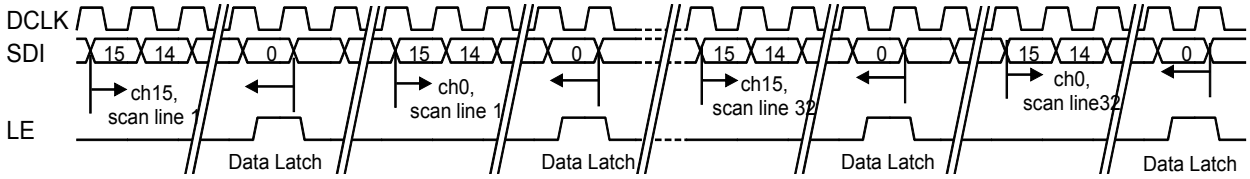

Figure 4. The timing diagram of 16-bit gray scale data

The 14- bit gray scale can be set through Bit [7]=1 in configuration register.

Example 2

Number of IC: 1

Number of scan lines: 32

Depth of PWM control: 14- bit

As shown in Figure 5, the data format is same as 16-bit gray scale data, only the last 2-bit (LSB) is "0".

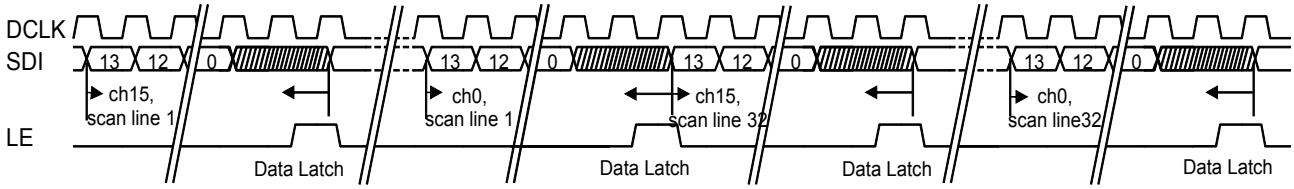

Figure 5. The timing diagram of 14-bit gray scale data

The gray scale data needs the GCLK to save the data into SRAM. The frequency of GCLK must be higher than 20% of DCLK to get the correct data.

After the last data latch command, it needs at least 50 GCLKs to read the gray scale data into internal display buffer before the Vsync command comes. And display is updated immediately until MBI5051/52/53 receives the Vsync signal (high pulse of LE pin is sampled by 3-DCLK rising edges), as figure 6 shows.

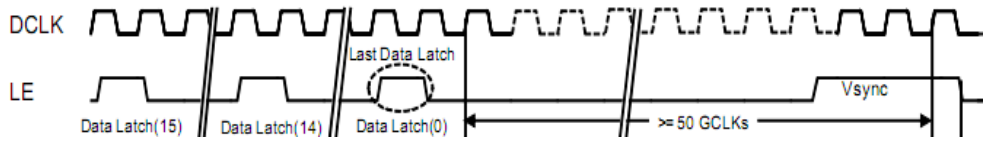

Figure 6. Vertical Sync

Section 3: The settings of gray scale data to the cascade of several MBI5051/52/53

If there are N pieces of MBI5051/52/53 in cascaded as Figure 7 shows, then the data length of each “data latch” will be 16 x N bits.

For one MBI5051/52/53, each latch needs 16-bits of grayscale data.

For two MBI5051/52/53 in cascaded, each latch needs 32-bits of grayscale data, and so on.

But no matter how many MBI5051/52/53 in cascaded, the latch signal only can be executed until all the data are ready, as figure 8 shows.

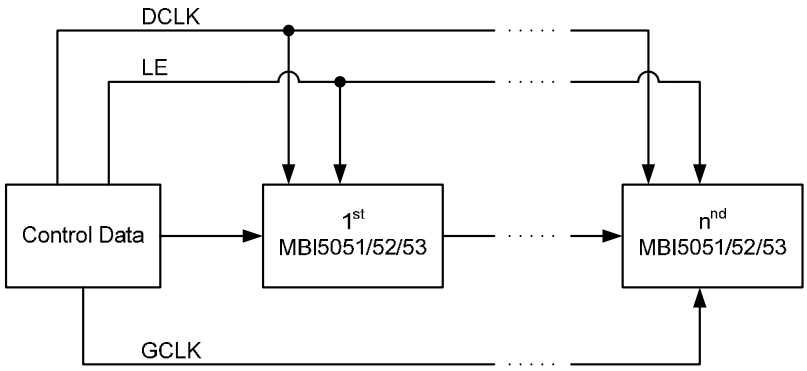

Figure 7. n pieces of MBI5051/52/53 in cascaded

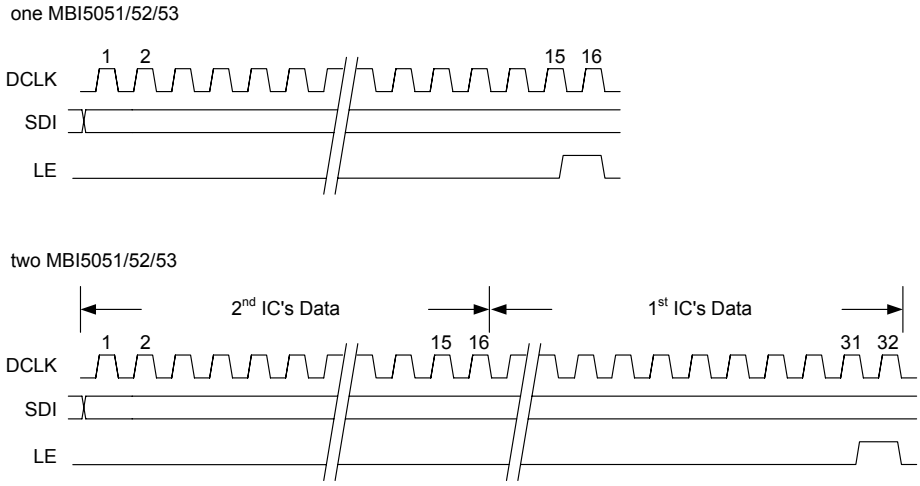

Figure 8. The timing diagram of “data latch” command

Section 4: Read/Write Configuration Register

MBI5051/52/53 embeds a readable and writeable configuration register which can determine the operation mode. The configuration register includes current gain adjustment, ghost-cancelling, and etc.

Figure 9 shows the control command of write configuration. Pre-Active command (high pulse of LE pin is sampled by 14-DCLK rising edges) must be executed before the write configuration command, and then the data can write into the configuration register. Each data length of MBI5051/52/53 is 16-bit, if there are N pieces of IC in cascaded, the 16xN bits date, which is forward counting from the LE falling edge, will be latched into the configuration register.

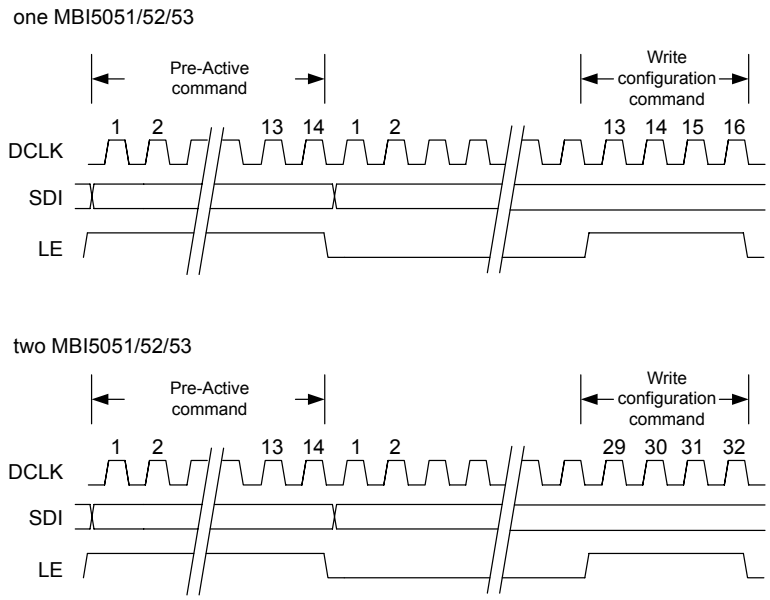

Figure 9. The waveform of writing data into configuration register

The data sequence starts from 2nd MBI501/52/53, and then the 1st IC. Each data starts from MSB. In the durations of Pre-Active command and Write Configuration command, LE must pull to low to prevent leaving the Pre-Active mode and the configuration data becomes invalid.

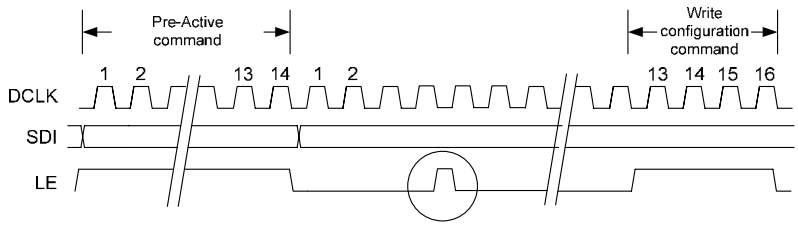

Figure 10. Example of incorrect LE signal - 1

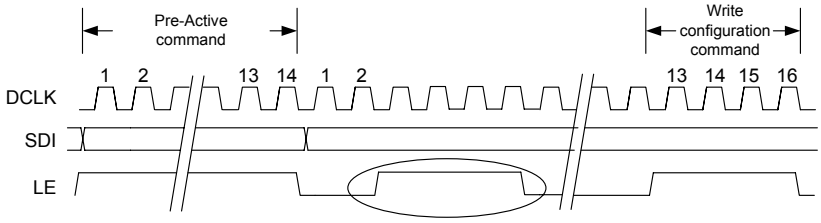

Figure 11. Example of incorrect LE signal - 2

Figure 13 shows the control command of Read Configuration. Any moment, once the LE high pulse is sampled by 5-DCLK rising edges, the first bit in configuration register will be outputted from SDO, and then each bit comes out with DCLK.

The sequence of read data starts from 2nd MBI5051/52/53, and then the 1st IC. In the duration of Read Configuration, the SDI signal can be ignored.

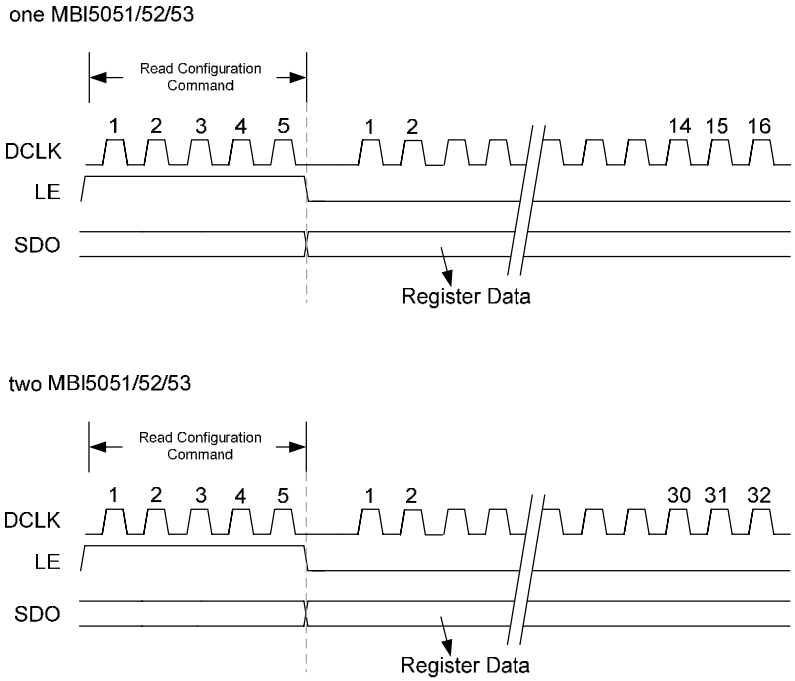

Figure 12. The diagram of reading data from configuration register

Section 5: Send Data and Display Image

MBI5051/52/53 embeds 4/8/16k-bit SRAM and divides it into two banks to reading and writing data frame. As figure 13 shows, the gray scale data of next frame can be sent while current frame is playing. After receive the Vsync command, the SRAM will switch the function of these two banks to reading and writing.

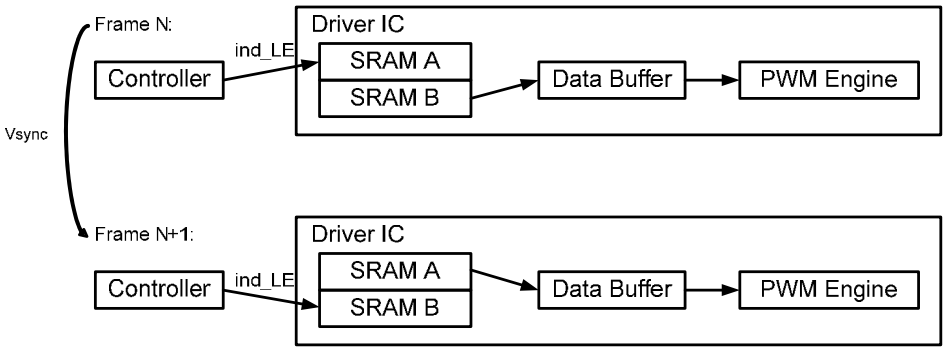

Figure 13. The data transmission structure of MBI5051/52/53

Section 6. Visual Refresh Rate and GCLK Multiplier Technology

With Scrambled-PWM (S-PWM) technology, MBI5051/52/53 enhances pulse width modulation by scrambling the “on” time into several small “on” periods. Thus the technology increases the visual refresh rate. The data refresh rate and pulse width in different image data can be calculated from the following formals.

Visual Refresh Rate

With Scrambled-PWM technology, the 65536 GCLKs (16-bits) PWM cycle of MBI5051/52/53 is divided into 64 sections, each section has 1024 GCLKs. The 16384 GCLKs (14-bit) PWM cycle of MBI5051 is divided into 16 sections, each section has 1024 GCLKs. The 16384 GCLKs (14-bit) PWM cycle of MBI5052/53 is divided into 32 sections, each section has 512 GCLKs.

The formulas of visual refresh rate are

In 16-bit S-PWM mode, visual refresh rate $F_{visual} = F_{GCLK} / [(1024 + t_{Dead}) \times N]$ ..... (1)

In 14-bit S-PWM mode, visual refresh rate $F_{visual} = F_{GCLK} / [(512 + t_{Dead}) \times N]$ ..... (2)

where

F_{visual}: Visual Refresh Rate.

F_{GCLK}: Gray Scale Clock Frequency.

t_{Dead}: Dead Time.

N: Number of Scan Lines.

For example, in the 32:1 time multiplexing application, whose driver is MBI5053, a 16-bit SPWM driver, the GCLK frequency is 15MHz, then the visual refresh rate could be calculated as below

F_{visual} =15MHz/[(1024+10)x32]=453

The MBI5051/52/53 provides a SRAM to save the frame data, the updated data transmission has to be completed before next frame. The GCLK frequency needn't to follow the frame rate.

For example, if MBI5053's GCLK is 15MHz, the dead time is 10 GCLK. The cycle number of GCLK=15MHz in a period is shown as table 1.

Table 1. The cycle numbers of GCLK=15MHz in a period

Case	Bit numbers of gray scale control(bit)	Frame rate (Hz)	Duty cycle of multiplexing design	Cycle number of GCLK counter in a period T_{DATA}
1	16	60	1/32 duty	7
2	16	50	1/16 duty	18
3	14	60	1/32 duty	14
4	14	50	1/16 duty	35

If the driver with 16-bit gray scale data, it needs 64 cycle number to complete a frame data. That means both case 1 and 2 don't have enough time to complete a frame data transmission. Increase the GCLK frequency of reduce the scan line is helpful to achieve this mission. Also, if the driver with 14-bit gray scale data, it needs 32 cycle number to complete a frame data. From above table, only case 4 can achieve this mission.

GCLK Multiplier Technology

If GCLK multiplier is enabled, GCLK will be dual edge triggered, that means the cycle time can be reduced by half. Table 2 shows the results of GCLK multiplier enabled.

Table 2. The cycle number of GCLK=15MHz when GCLK multiplier enabled

Case	Bit numbers of gray scale control(bit)	Frame rate (Hz)	Duty cycle of multiplexing design	Cycle number of GCLK counter in a period T_{DATA}
1	16	60	1/32 duty	15
2	16	50	1/16 duty	36
3	14	60	1/32 duty	29
4	14	50	1/16 duty	71

The Bits 15~7 are used to define the refresh rate (the SDI must larger than 64). The minimum output pulse width is the reciprocal of GCLK frequency.

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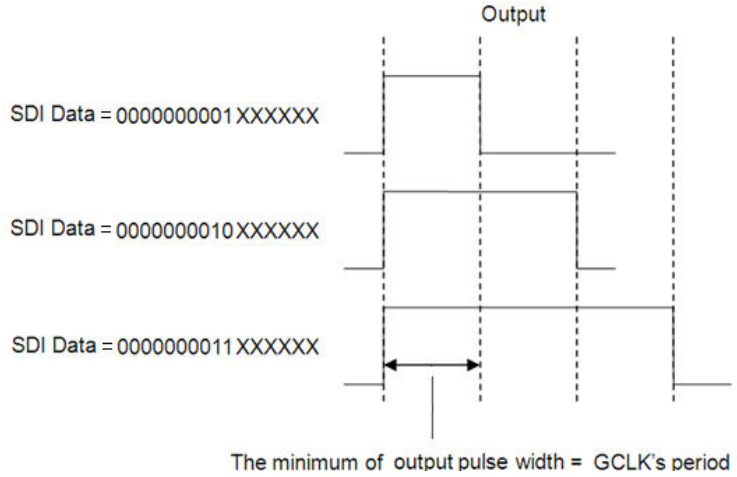

Figure 14. The diagram of SDI data and pulse width

Section 7: The Maximum Cascaded Number of MBI5051/52/53

The frame data must be updated in a picture period. Therefore, the maximum cascaded number of MBI5051/52/53 is decided by DCLK frequency and scan lines, and it can be calculated from the following equation

$$N = (F_{DCLK} \times duty) / (\text{the amount of data bit} \times \text{frame rate}) \quad \text{..... (3)}$$

For example, if the frame rate is 60 times/s, DCLK frequency is 15MHz, and duty is 1/16. Then from (3), the maximum cascaded number of MBI5051/52/53 is $N = [(15 \times 10^6) \times (1/16)]/(16 \times 16 \times 60) = 61$. Table 3 shows the maximum cascaded number of MBI5051/52/53 under different conditions.

Table 3. The maximum cascaded number of MBI5051/52/53 at DCLK=15MHz

Case	Frame rate (Hz)	Duty cycle of T_{DATA}	The maximum cascaded number of MBI5051/52/53
1	60	1/4 duty	244
2	60	1/8 duty	122
3	60	1/16 duty	61
4	60	1/32 duty	30
5	50	1/4 duty	292
6	50	1/8 duty	146
7	50	1/16 duty	73
8	50	1/32 duty	36

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Section 8: Current Gain

MBI5051/52/53 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, it should be controlled in the output current range of MBI5051/52/53; otherwise, the over designed output current can't be guaranteed.

The Bit 5 to Bit 0 in configuration register is used to set the current gain, and the defaulted gain code is 6'b101011. The Bit 5 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-					HC	DA4	DA3	DA2	DA1	DA0
Default	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1

6 bit gain code data

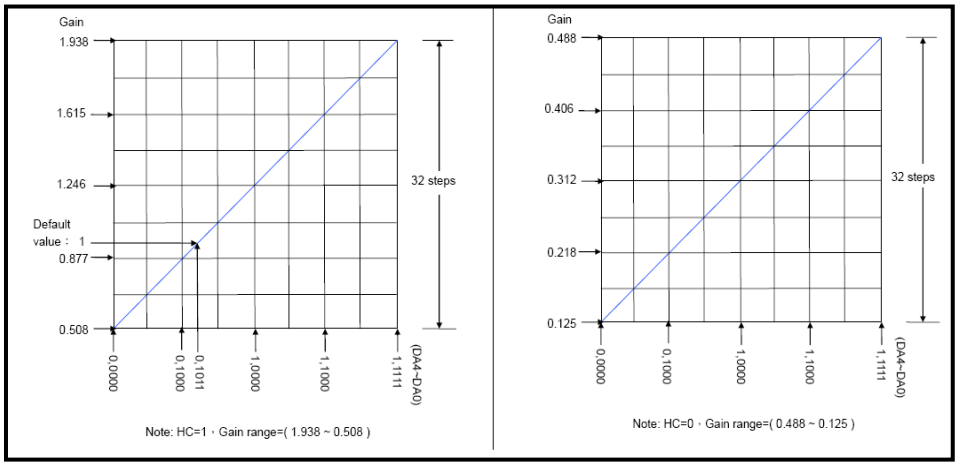

Figure 15. The relationship of current gain and gain code

The R_{ext} can be calculated by following equation

$$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 23.0 \quad \text{..... (4)}$$

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

HC=1, D=(65xG-33)/3 ..... (5)

HC=0, D=(256xG-32)/3 ..... (6)

Example 1

If I_{OUT} =20mA and G=1, then the gain code is

Step 1: From (4), the R_{ext} = [(0.61 × 1) / 20mA] × 23 = 701.5Ω. From figure 15, G=1 in the high gain region, that means the HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary, D=01011, therefore DA[4:0]= 01011.

The 6 bits (bit 5~bit 0) of the configuration register are 6'b101011.

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Example 2

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 30mA, then

Step 1: G= 30mA /20mA =1.5 (HC=1).

Step 2: From (5), D= (65x1.5-33)/3=21.5≒ 22.

Step 3: Convert D into binary, D=01011, therefore DA[4:0]= 5'b10110.

Step 4: The adjusted gain code is 6'b110110.

Example 3

If R_{ext} is 701.5Ω, the adjusted output current is from 20mA to 5mA, then

Step 1: G= 5mA /20mA =0.25 (HC=0).

Step 2: From (6), D= (256x0.25-32)/3=10.67≒ 11.

Step 3: Convert D into binary, D=01011, therefore DA[4:0]= 5'b01011.

Step 4: The adjusted gain code is 6'b001011.

Figure 16 is the relationship of output current and gain data under V_{DD}=5.0V and R_{ext}=700Ω. The defaulted current gain, G =1, is corresponding to 20.6mA.

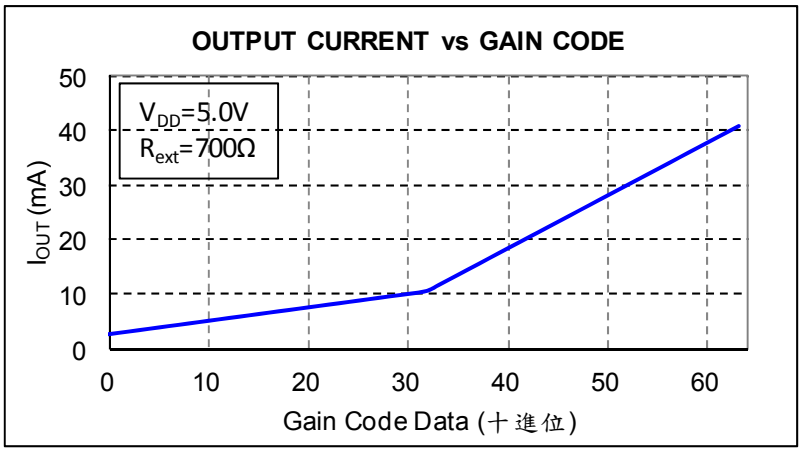

Figure 16. The relationship of current gain and code data under V_{DD}=5.0V and R_{ext}=700Ω.

Section 9: The Notice of LED Open-Circuit Detection

As figure 17 shows, MBI5051/52/53 executes the compulsory open-circuit detection while the LE high pulse is sampled by 7-DCLK rising edges. In the duration of compulsory open circuit detection, all the output channels will be turned off.

When LE high pulse pin is sampled by 1-DCLK rising edge, the result of open circuit detection will be shifted out from the SDO pin and the sequence is from MSB to LSB. The error detection will stop while the result is shifted out.

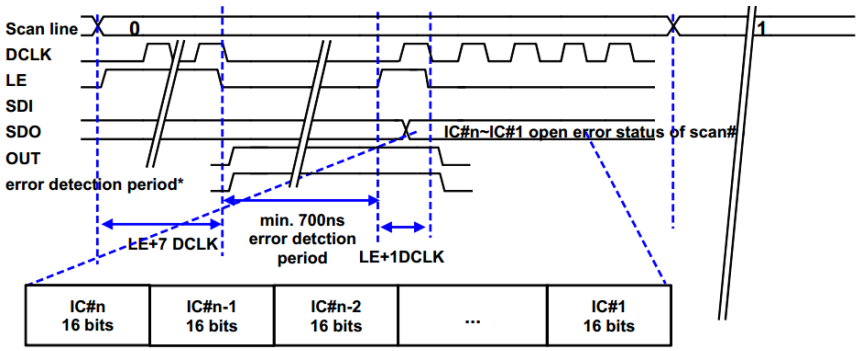

Figure 17. The timing waveform of compulsory error detection

In addition, please note the following items

1. In the duration of compulsory open circuit detection, the SDI data can be ignored until LE pin is sampled by 1-DCLK rising edge. The duration should be keep longer than 700ns, as figure 17 shows.
2. When output turns on, please make sure the output voltage (V_{DS}) is higher than 0.3V.
3. In the duration of compulsory open circuit detection, the scan line can't switch.
4. MBI5051/52/53 doesn't support LED short circuit deletion.
5. MBI5051/52/53 detects the LED open circuit once a scan line, however the detection result only can report which channel's LED is failed, can't exactly point out the failed LED in which scan line, this mission can be taken by controller.

Detected Result	Status
0	Open
1	Normal

Section 10: The Control Signal of Time Mulitplexing

Figure 18 shows an example of 4pcs MBI5053 in 32:1 time multiplexing application.

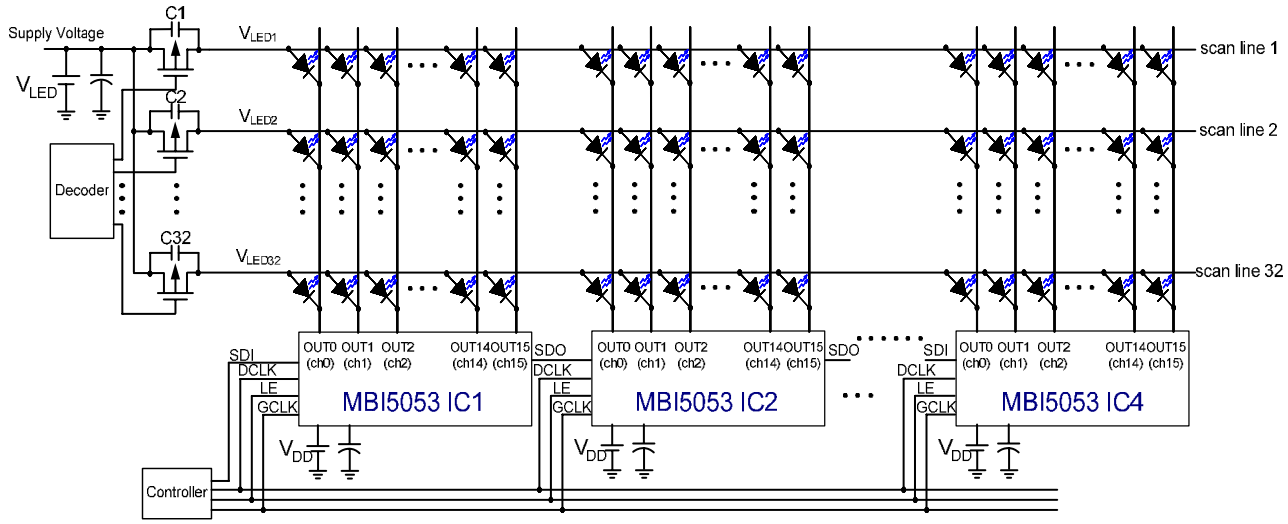

Figure 18. The schematic of time multiplexing application

In this example, the gray scale data is 2048 bits (4x16x32), and needs 512 times data latch (16x32).The Vsync command, which is used to update the frame data, should be executed at least 50 GCLK later than the last data latch. In the duration of Vsync command, the GCLK should be stopped.

Step 1. The Sequence of Gray Scale Data

Figure 19 shows the sequence of gray scale data. The bit63~bit48 are the gray scale data of 4th IC's /OUT15, and bit15~bit0 are the 1st IC's. A data latch command puts these data into SRAM buffer and then continue the data input of next output channel. After finish the data input of 1st scan line, then repeat above sequence to complete the others scan line's data.

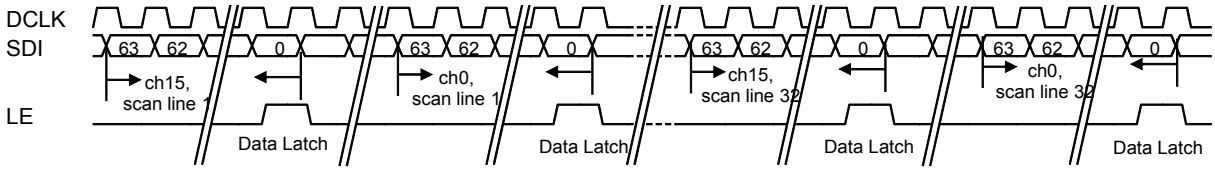

Figure 19. The sequence of gray scale data

Step 2. The Frame Data Update Command, Vsync GCLK≠DCLK

The Vsync command should be executed at least 50-GCLK later than the last data latch, the reason of this spent time is to read the gray scale data from SRAM. Figure 20 shows the limitations of Vsync command, and followings are the further explain.

a.) The GCLK should be stopped before the Vsync command. The hold and setup times must respectively meet the specifications of t_{SU2} and t_{H2} in datasheet.

b.) Dead time is the interval between each scan line, and it terminates when GCLK is acted. Since the frame data will be updated after Vsync command executed, the scan line should be switched from line 32 to line 1 to restart the new frame data.

c.) In the duration of dead time, the DCLK must be stopped, and don't execute the data latch command.

d.) In the duration of dead time, the new data will be loaded in the internal display buffer, and the data will be showed on after the dead time.

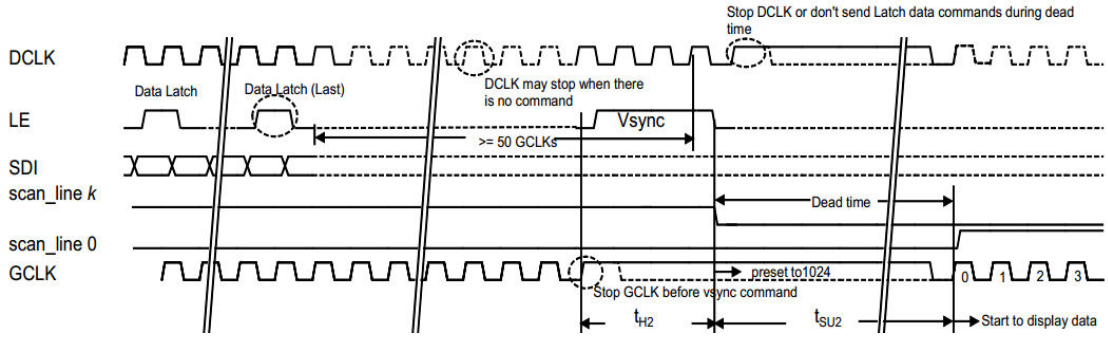

Figure 20. The timing waveform of Vsync (GCLK≠DCLK)

GCLK = DCLK

The differences from GCLK≠DCLK are

a.) Due to the GCLK=DCLK, the DCLK can't stop even the frame data and command have completed transmission.

b.) The DCLK has to stop after executed the Vsync command. The hold and setup times must respectively meet the specifications of t_{SU2} and t_{H2} in datasheet

c.) The DCLK must stop before the GCLK counter is 1023.

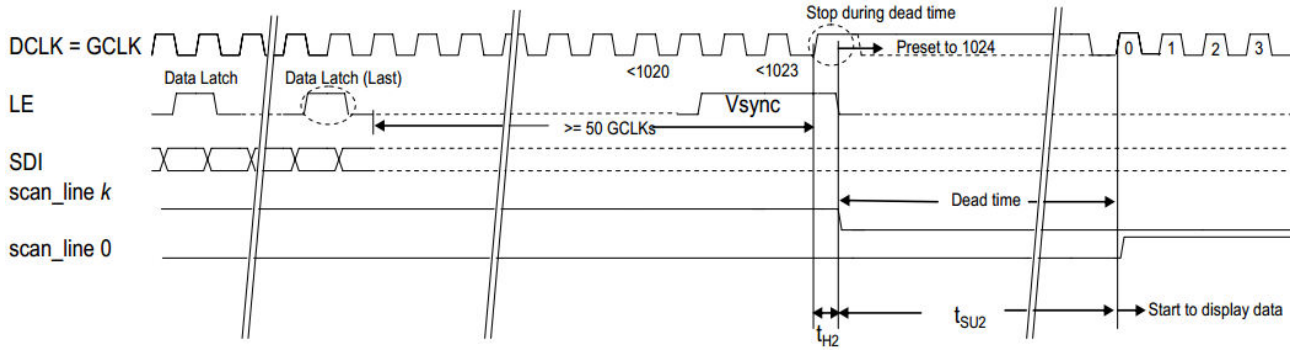

Figure 21. The timing waveform of Vsync (GCLK=DCLK)

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Step 3. Scan Line Switching

The gray scale data of MBI5051/52/53 are stored in the SRAM and use the technology of scrambled-PWM to improve the refresh rate. An extra GCLK is needed to switch the scan line when GCLK is counting from 0 to 1023. The dead time is determined by the duration of suspended GCLK. When the GCLK counter is 1024, all the output channels will be turned off in the dead time. Figure 22 shows the timing waveform.

Note: Once the amount of scan line is set in the status register, the amount of data string must same as the scan line to obtain normal display.

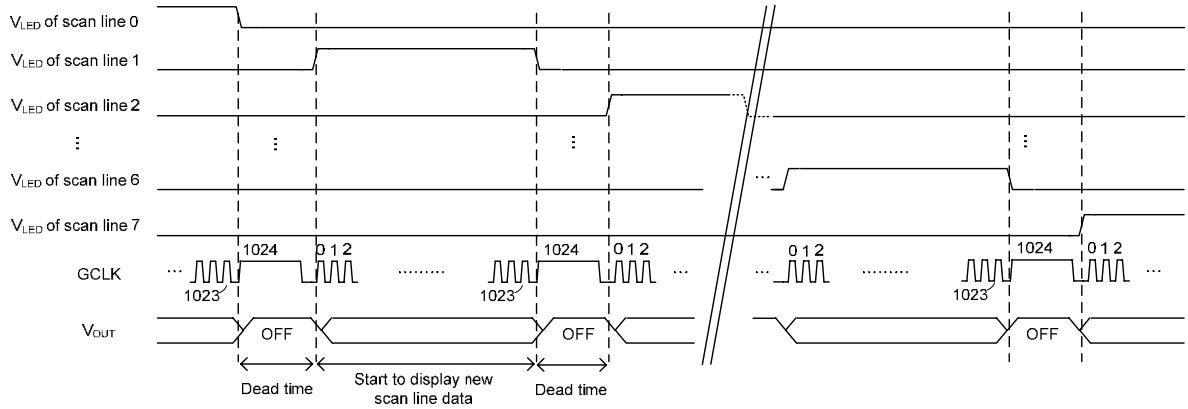

Figure 22. The timing waveform of switching scan line

Section 11. Ghost-Cancelling in the Time- Multiplexing LED Displays

The following actions can be taken to cancel the ghost effect in time multiplexing application.

Ghost-Cancelling

Figure 23 shows the diagram of the discharge/pre-charge circuit to cancel the ghost effect. The LEDs are turned on by the sequence of LED 0-0, LED 1-1⋯, LED n-15.

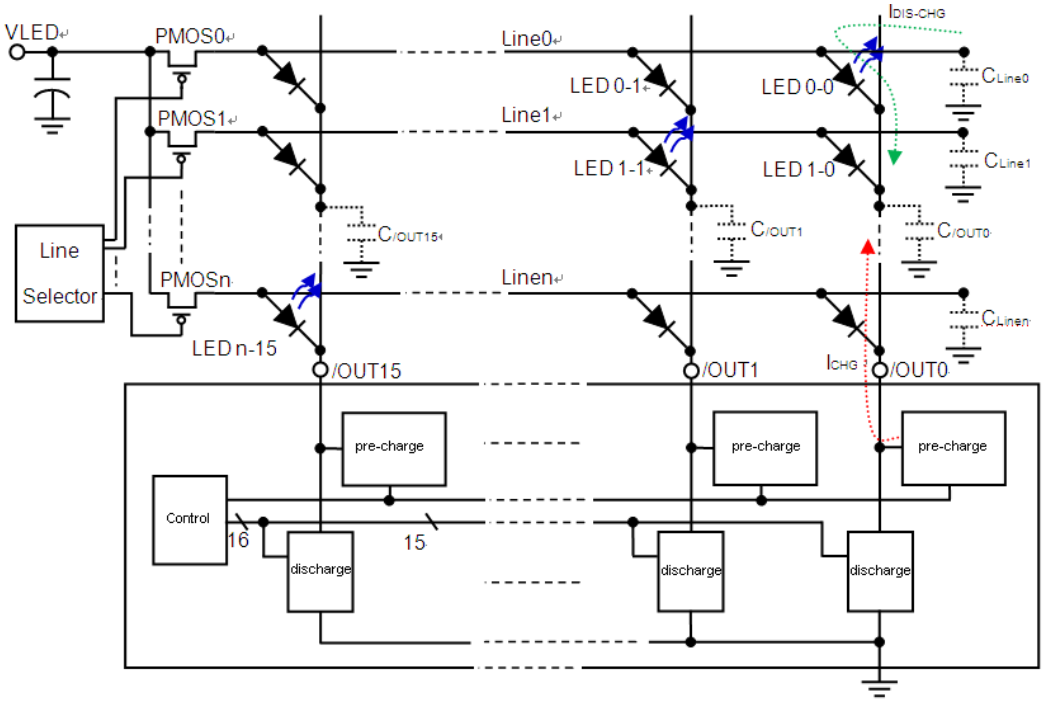

Figure 23. The diagram of the discharge/pre-charge circuit to eliminate the ghost effect

Ghost-Cancelling

The integrated ghost-cancelling feature can relieve the ghosting effect in time multiplexing LED display. The Bits E and F in status register are used to enable the functions, and figure 25 shows the timing waveform. An additional GCLK has to be inserted to present the dead time. To keep all the PMOS off while switching the scan lines. The high level of the additional GCLK determines the period of upper ghost-cancelling, and the low level is for lower ghost-cancelling.

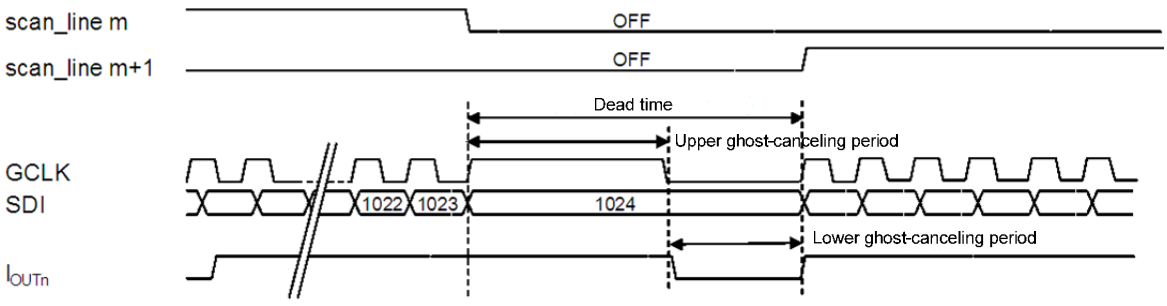

Figure 25. The timing waveform of upper and lower ghost-canceling

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When the ghost effect is happened in the time multiplexing LED display, enable both the Bit E and Bit F are recommended. Figure 26 is the display which hasn't enabled the ghost-cancelling function, and figure 27 is the enabled. In figure 27, the ghost effect has been complete cancel.

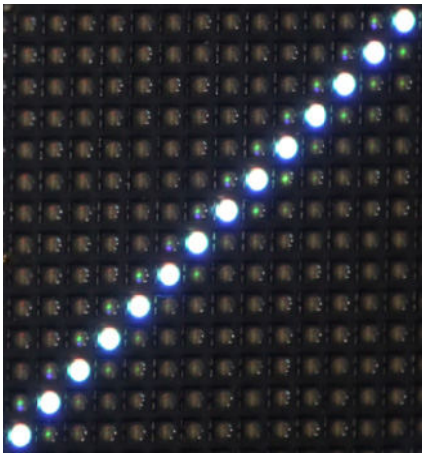

Figure 26. The display of disable upper/lower ghost cancelling

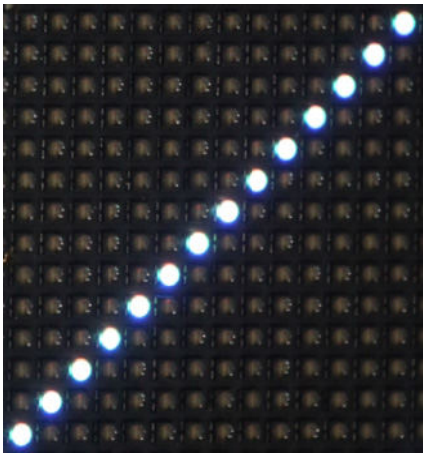

Figure 27. The display of enable upper/lower ghost cancelling

Section 12: Software Reset

When the software reset command is enabled, the internal counters of GCLK and data latch will be reset, and turned off all the output channels. However, the gray scale data stored in the SRAM, configuration register and current gain won't be reset.

Summary

MBI5051/52/53 uses the embedded S-PWM to control LED current and provides a storage solution of 4/8/16k-bit SRAM. Users don't need to send new data every time. This article provides the design guideline for uses.

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MBI5152 Application Note

Forward

MBI5152 features an embedded 8k-bit SRAM, which can support up to 1:16 time-multiplexing application. Users only need to send the whole frame data once and to store in the embedded SRAM of LED driver, instead of sending every time when the scan line is changed; therefore it can easily achieve high grayscale with slow DCLK frequency. This article provides the application information of MBI5152, such as the input method of image data and the setting of gray scale data. The detail operations are described in the following sections.

Time-multiplexing Application Design

Figure 1 shows the 3pcs cascaded MBI5152 in 1:16 time multiplexing application.

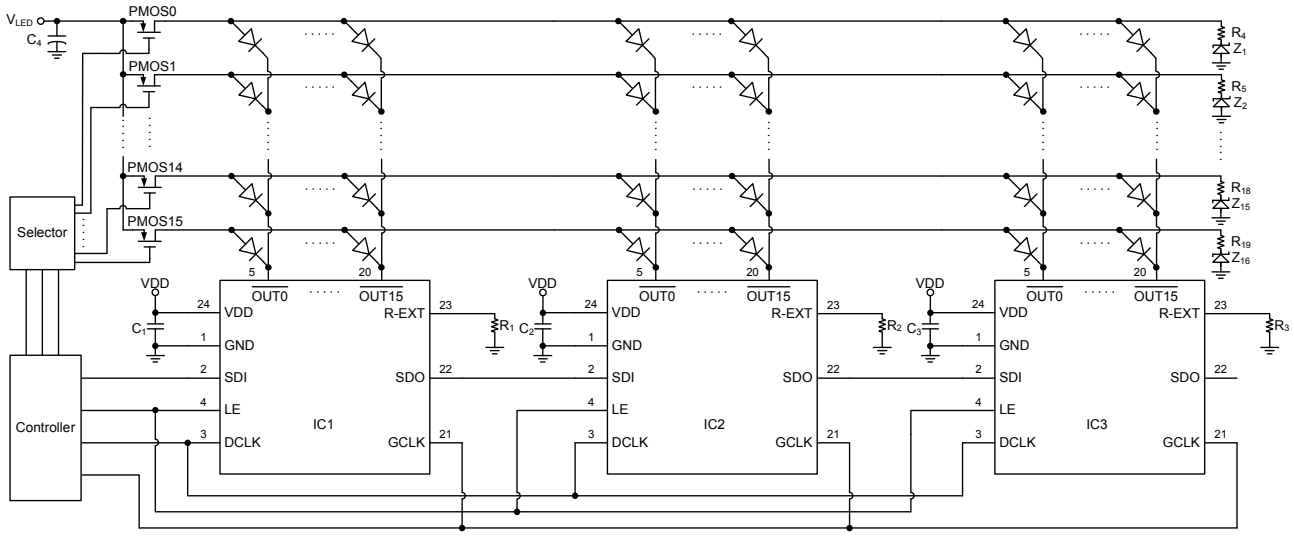

Figure 1. 3pcs cascaded MBI5152 in 1:16 time multiplexing application

Section 1: The Setting of Configuration Register

The setting of configuration data is described as below.

1. The “Pre-Active” command, LE arrested 14-DCLK rising edges, must be announced before “write configuration” command.
2. The data sequence of cascaded IC is ICn→ICn-1→…→IC2→IC1。
3. The sequence of gray scale data is bit15→bit14→…→bit1→bit0。
4. If there are N pcs of MBI5152 in cascaded, then the data length of each “data latch” will be 16 x N bits.
5. When LE is asserted 4-DCLK rising edges, serial data are written to the configuration register 1. When LE is asserted 8-DCLK rising edge, serial data are written to the configuration register 2.
6. The control signals shouldn’t come out until the power of driver board is stable.
7. To ensure the command is valid, the LE false trigger should be avoided in the interval between pre-active and write configuration.

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For lower ghost elimination, the configure registers, which are shown in table 1 and 2, are recommended.

Table 1. The recommended configuration register 1 for lower ghost elimination

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	1

Where, bitB~bit0 can be adjusted by display specifications.

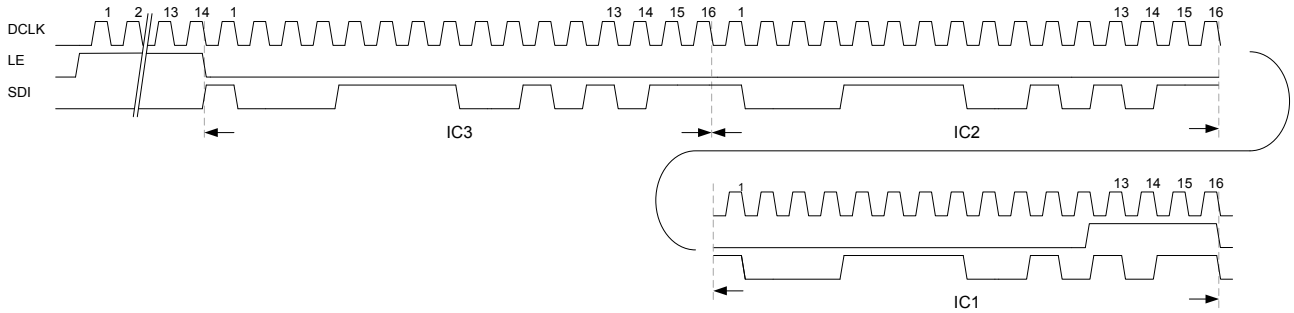

Figure 2. Example of Configuration register 1 setting for 3pcs cascaded MBI5152

Table 2. The recommended configuration register 2 for lower ghost elimination

The setting of configuration register 2 for R-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1

The setting of configuration register 2 for G-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	0	0	0	1	0	1	0	1

The setting of configuration register 2 for B-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	0	0	0	0	0	1	0	1	0	1

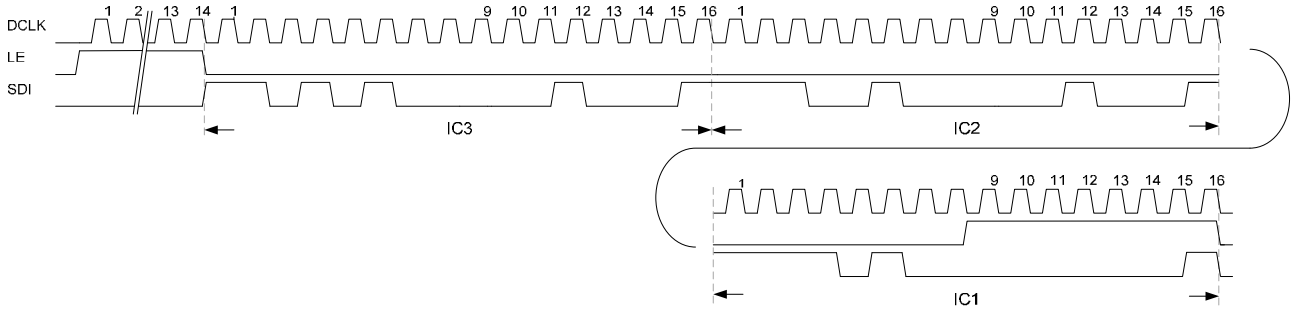

Figure 3. Example of Configuration register 2 setting for 3pcs cascaded MBI5152

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Section 2: The Setting of Gray Scale

The setting of gray scale data describes as below.

1. The sequence of input data starts from scan line 1→ scan line 2→…. → scan line M-1→ scan line M (M≦16)
2. The data sequence of cascaded IC is ICn→ICn-1→…. →IC2→IC1.
3. The data sequence of each channel is ch15→ch14→…. →ch0.
4. The data length of each channel is 16-bits, and the default PWM mode is 16-bits. The sequence of gray sacle is bit15→bit14→bit13…→bit0 as figure 4 shows. The 14-bits gray scale can be set through Bit[7]=1 in configuration register 1, and the sequence of gray scale data is bit13→bit12→…→ bit0→ 0→ 0, the last 2-bits (LSB) are set to “0”.
5. The frequency of GCLK must be higher than 20% of DCLK to get the correct gray scale data.
6. LE executes the data latch to send gray scale data into SRAM. Each 16xN bits data needs a “data latch command”, where N means the number of cascaded driver.
7. After the last data latch, it needs at least 50 GCLKs to read the gray scale data into internal display buffer before the Vsync command comes.
8. Display is updated immediately when MBI5152 receives the Vsync signal.
9. GCLK must keep at low level more than 7ns before MBI5152 receives the Vsync signal.
10. The period of dead time (ie. The 1025th GCLK) must be larger than 100ns.

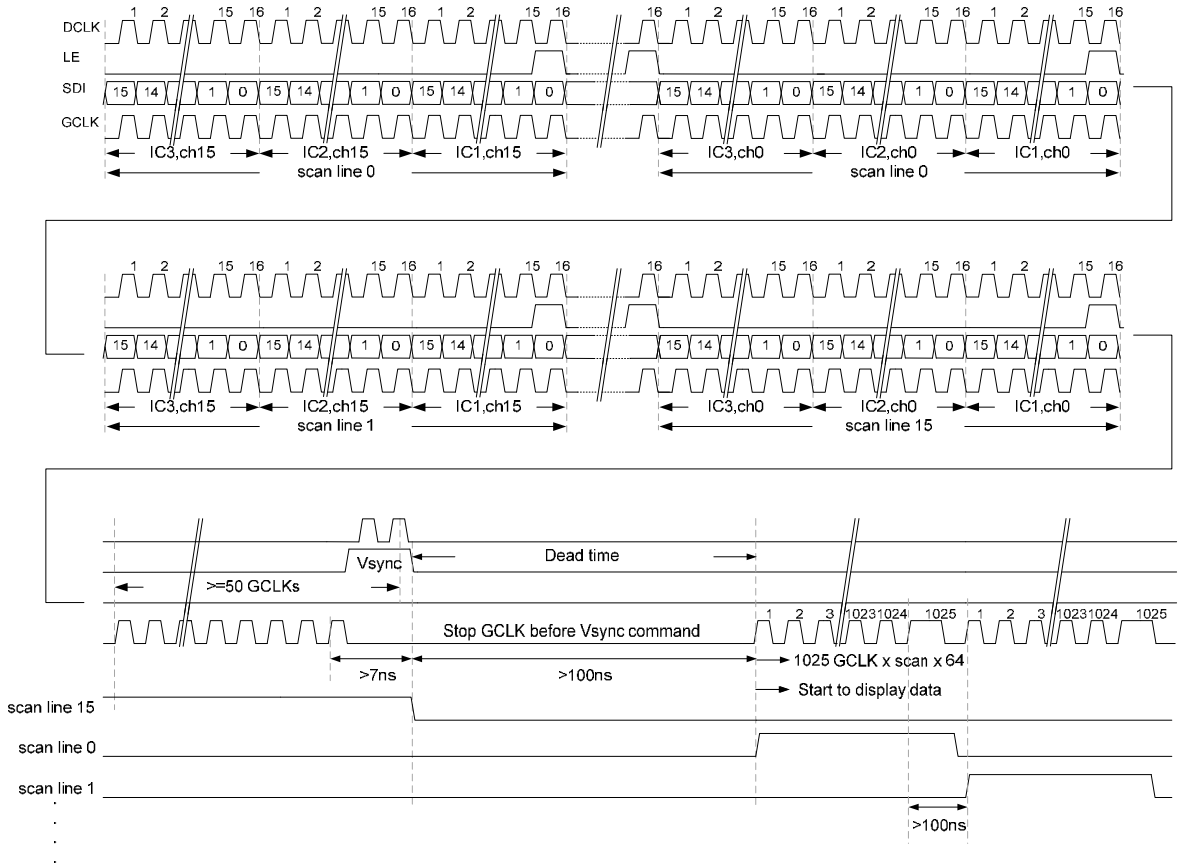

Figure 4. The timing diagram of 16-bit gray scale data

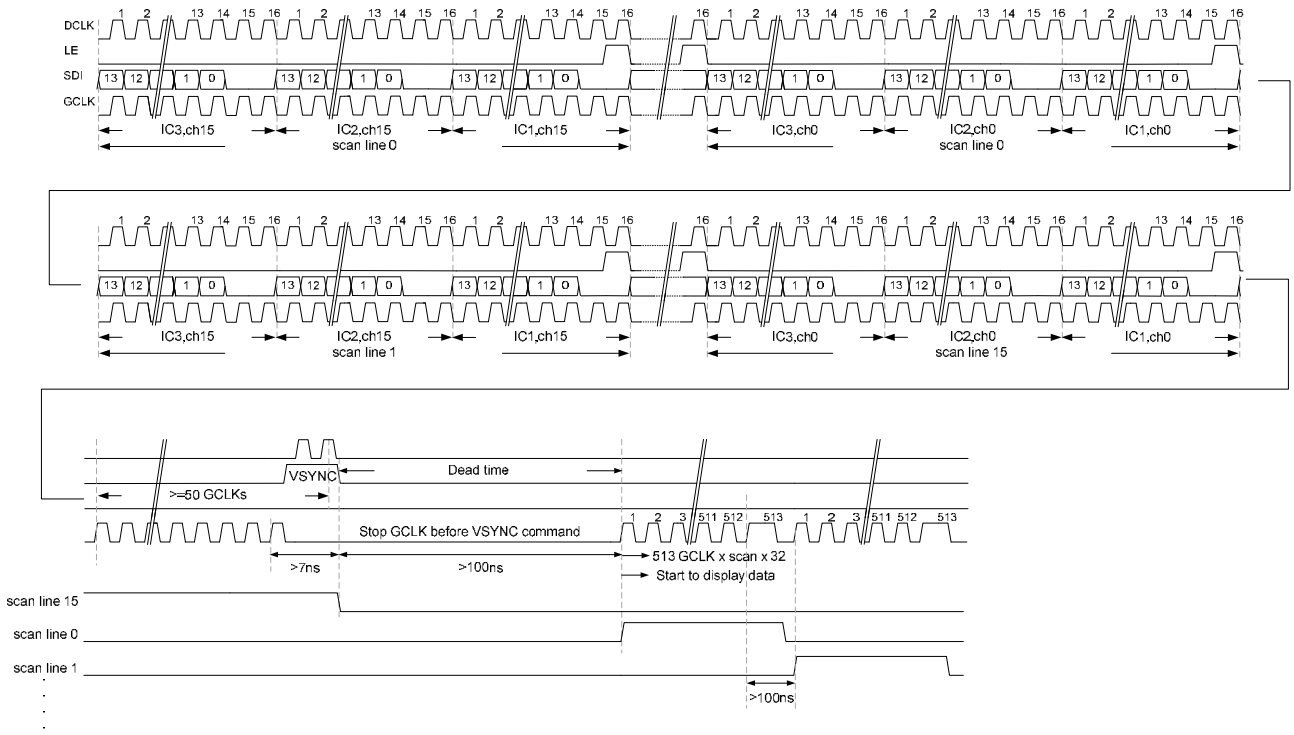

Figure 5. The timing diagram of 14-bit gray scale data

Section 3: Read configuration Register

The setting of read configuration register describes as below.

1. The command to read the configuration register 1 is LE arrested 5-DCLK rising edges, and LE arrested 90DCLK rising edges is to read the configuration register 2.
2. Configuration register data will be outputted from SDO, and each bit comes out with DCLK.
3. It needs16 x N of DCLK to send configuration register data, where N means the number of cascaded driver.
4. The read out sequence of cascaded IC is ICn→ ICn-1→…. →IC2→IC1.
5. The bit read out sequence is bit15→bit14→…. →bit1→bit0。
6. In the duration of read configuration, the SDI signal can be ignored.
7. Read out the configuration register data in non-display state is recommended.

Figure 6 shows the example of reading configuration register 1 in 3pcs cascaded MBI5152 .

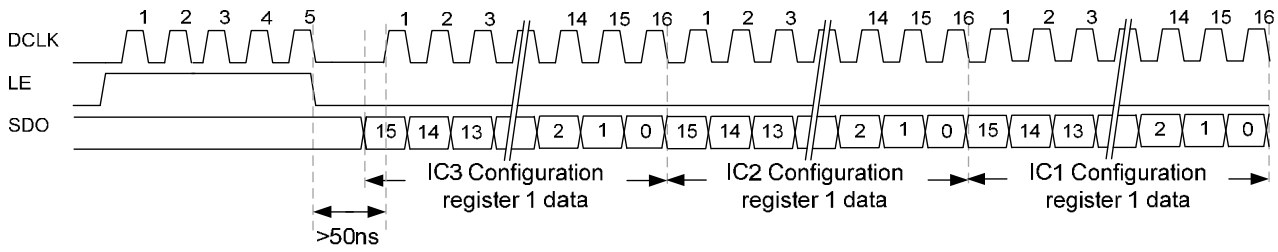

Figure 6. Example of reading configuration register 1 in 3pcs cascaded MBI5152

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Figure 7 shows the example of reading configuration register 2 in 3pcs cascaded MBI5152.

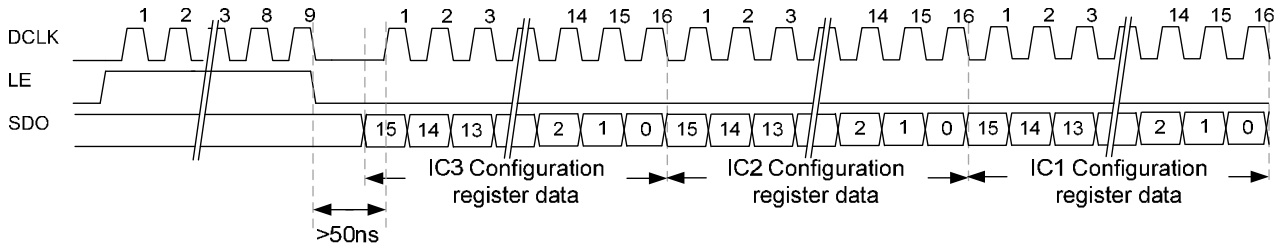

Figure 7. Example of reading configuration register 2 in 3pcs cascaded MBI5152

Section 4: Send Data and Display Image

MBI5152 embeds 8K-bit SRAM and divides it into two banks, SRAMA and SRAMB to reading and writing data frame. , SRAMB is used to play the current frame data, and SRAMA receives the gray scale data of next frame. After receive the Vsync command, the assignments of these two SRAM will be exchanged, as figure 8 shows.

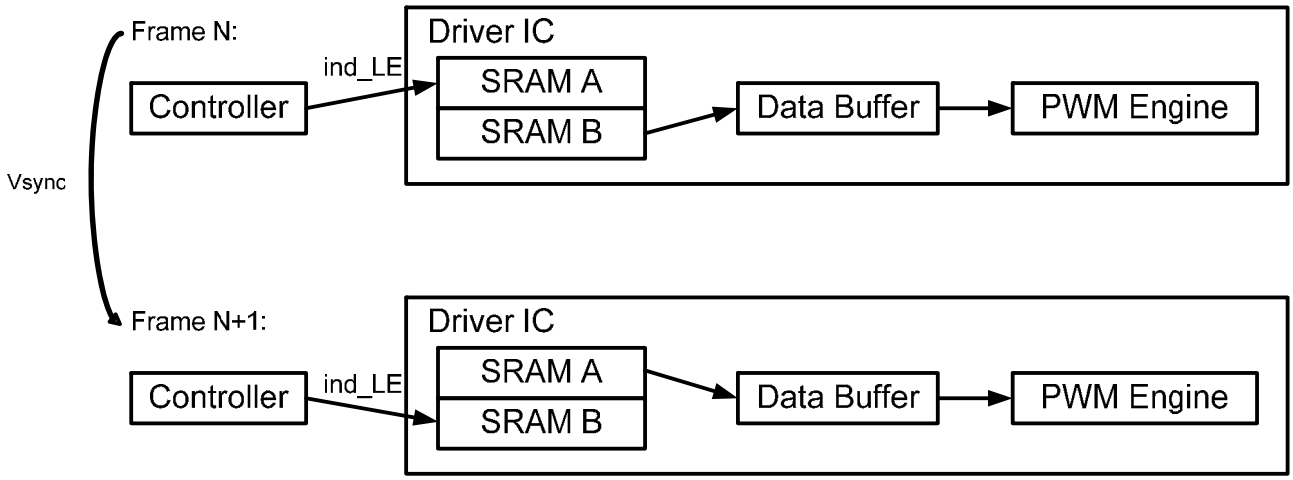

Figure 8. The data transmission structure of MBI5152

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Section 5: Visual Refresh Rate and GCLK Multiplier Technology

Visual Refresh Rate

With S-PWM technology, the 16-bits PWM cycle of MBI5152 is divided into 64 sections, and each section has 1024 GCLKs. The 14-bits PWM cycle of MBI5152 is divided into 32 sections, and each section has 512 GCLKs. The formulas of visual refresh rate are

In 16-bits S-PWM mode, visual refresh rate $F_{visual} = \frac{1}{[1024 \times (1/F_{GCLK}) + t_{Dead}] \times N}$ (1)

In 14-bits S-PWM mode, visual refresh rate $F_{visual} = \frac{1}{[512 \times (1/F_{GCLK}) + t_{Dead}] \times N}$ (2)

where

F_{visual}: Visual Refresh Rate.

F_{GCLK}: Gray Scale Clock Frequency.

t_{Dead}: Dead Time.

N: Number of Scan Lines.

For example, for 16-bits PWM mode, the 1:16 time-multiplexing application with 15MHz GCLK frequency and the dead time is 10-GCLKs, the visual refresh rate could be calculated as below

$$F_{visual} = \frac{1}{[(1024+10) \times (1/15MHz)] \times 16} = 906(Hz)$$

Since the frame data can be stored in the embedded SRAM of MBI5152, the updated data only need to complete transmission before next frame. The GCLK frequency needn't to follow the frame rate. If MBI5152's GCLK is 15MHz, the dead time is 10 GCLKs, table 3 shows the limitation of in each case.

Table 3. The limitation in different cases when GCLK=15MHz

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	16	60	15
2	16	8	50	36
3	14	16	60	29
4	14	8	50	71

If the driver with 16-bits gray scale data, it needs 64 cycles to complete a frame data. That means both case 1 and 2 don't have enough time to complete a frame data transmission. Also, in 14-bits gray scale data, it needs only 32 cycles to complete a frame data. Case 3 doesn't have enough time to complete a frame data transmission. From above table, only case 4 can achieve this mission.

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GCLK Multiplier Technology

If GCLK multiplier is enabled, GCLK will be dual edge triggered, that means the cycle time can be reduced by half, and the cycle number of GCLK counter in a period time will be double. Table 4 shows the results of GCLK multiplier enabled.

Table 4. The limitation in different cases when GCLK=15MHz (GCLK multiplier enabled)

Case	Bit numbers of gray scale control (bit)	Scan line	Frame rate (Hz)	Cycle number of GCLK counter in a period T_{DATA}
1	16	16	60	29
2	16	8	50	71
3	14	16	60	58
4	14	8	50	140

As MBI5152 GCLK multiplier is enabled, case 2, 3 and 4 can complete a frame transmission in 16-bits and 14-bits PWM mode respectively.

Take the 16-bit gray scale data for example, the Bits 15~7 are used to define the refresh rate (the SDI must larger than 64). The minimum output pulse width is the reciprocal of GCLK frequency.

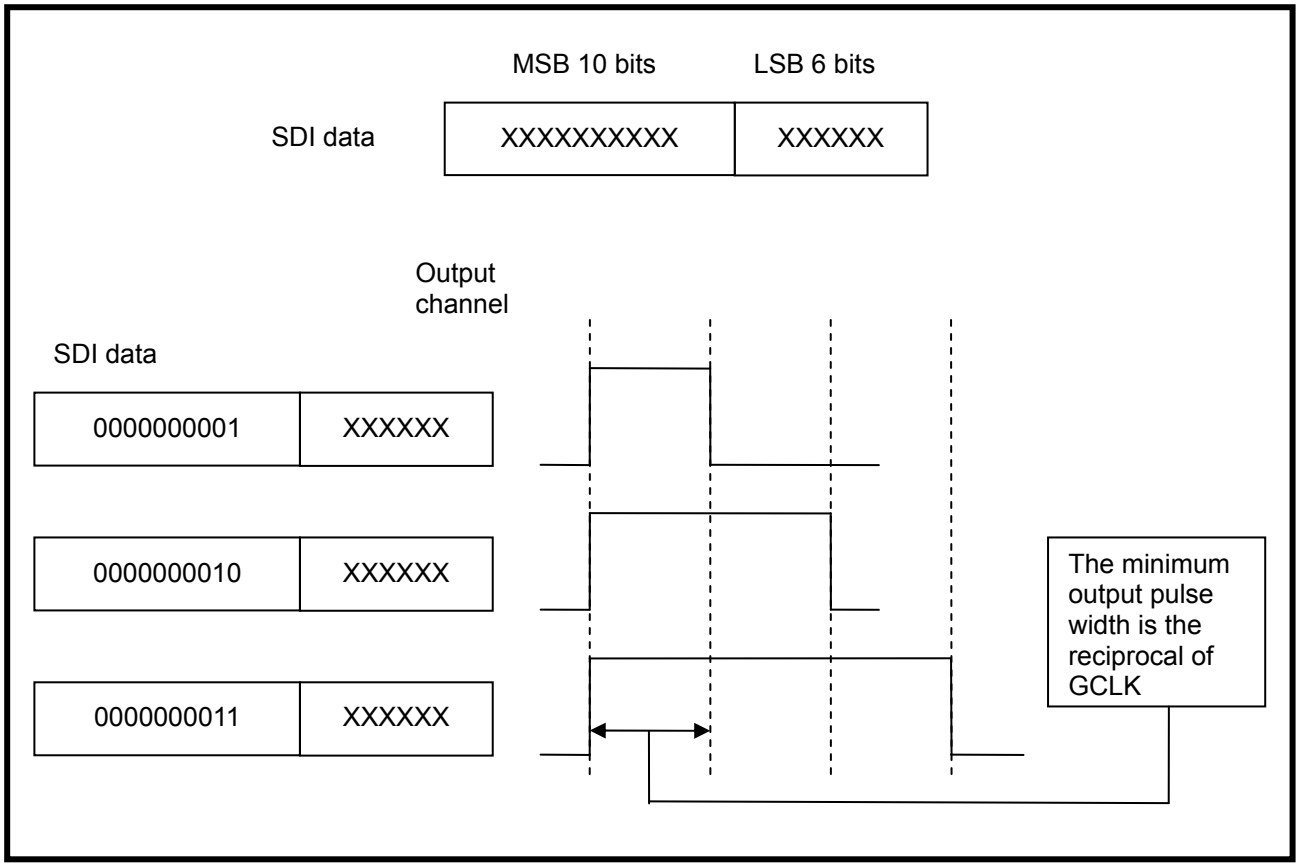

Figure 9. The diagram of SDI data and pulse width

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Section 6: The Maximum Cascaded Number of MBI5152

The frame data must be updated in a picture period. Therefore, the maximum cascaded number of MBI5152 is decided by DCLK frequency and scan lines, and it can be calculated from the following equation

$$N = F_{DCLK} / (\text{the amount of data bit x scan line x frame rate}) \quad (3)$$

Take the case 3 in table 5 for example, if the frame rate is 60 times/s, DCLK frequency is 15MHz, 1:16 time-multiplexing application, then from (3), the maximum cascaded number of MBI5152 is

$$N = (15x10^6) / [(16 \times 16) \times 16 \times 60] = 61$$

Table 5. The maximum cascaded number of MBI5152 at DCLK=15MHz

Case	Bit numbers of gray scale control (bit)	Frame rate (Hz)	Scan line	The maximum cascaded number
1	16	60	4	244
2	16	60	8	122
3	16	60	16	61
4	16	50	4	292
5	16	50	8	146
6	16	50	16	73

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Section 7: Current Gain Adjustment

MBI5152 current gain can be adjusted from 12.5% (default) to 200%. No matter the output current is set by Rext or current gain, the adjusted current must keep in the constant current range of MBI5152. For example, after current gain adjustment, the output current must in the range of 1mA~20mA when V_{DD}=5.0V or 1mA~10mA when V_{DD}=3.3V. Otherwise, the over designed output current can't be guaranteed.

The Bit 5 to Bit 0 in configuration register 1 is used to set the current gain, and the defaulted gain code is 6'b101011. The Bit 5 is HC bit, HC=0 means in low current region, and HC=1 is high current region.

Table 6. The setting of current gain

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Define	-	-	-	-	-	-					HC	DA4	DA3	DA2	DA1	DA0
Default	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1
											← 6 bits current gain setting →					

The R_{ext} can be calculated by following equation

$$R_{ext} = (V_{R\text{-}EXT} / I_{OUT}) \times 24 \quad \text{.....(4)}$$

where $V_{R\text{-}EXT}$ = 0.61Volt ×G, and G means the current gain.

The relationship of current gain (G) and gain data (D) is

HC=1, D=(65xG-33)/3 .....(5)

HC=0, D=(256xG-32)/3 .....(6)

Example 1

If I_{OUT} =10mA and G=1, then the gain code is

Step 1: From (4), the R_{ext} = [(0.61 × 1) / 10mA] × 24 = 1464Ω. From figure 10, G=1 in the high gain region, that means the HC=1. Thus, substitute above information into (5), the D=(65xG-33)/3=10.67≒11.

Step 2: Convert D into binary, D=01011, therefore DA[4:0]= 01011.

The 6 bits (bit 5~bit 0) of the configuration register are 6'b101011.

Example 2

If R_{ext} is 1464Ω, the adjusted output current is from 10mA to 18mA, then

Step 1: G= 18mA /10mA =1.8 (HC=1).

Step 2: From (5), D= (65x1.8-33)/3=28.

Step 3: Convert D into binary, D=11100, therefore DA[4:0]= 5'b11100.

Step 4: The adjusted gain code is 6'b111100.

Example 3

If R_{ext} is 1464Ω, the adjusted output current is from 10mA to 3mA, then

Step 1: G= 3mA /10mA =0.3 (HC=0).

Step 2: From (6), D= (256x0.3-32)/3=14.9≒ 15.

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Step 3: Convert D into binary, D=01111, therefore DA[4:0]= 5'b01111.

Step 4: The adjusted gain code is 6'b001111.

Figure 10 shows the relationship of current gain and gain code. The defaulted gain code of MBI5152 is 6'b101011, is corresponding to 1.015 current gain.

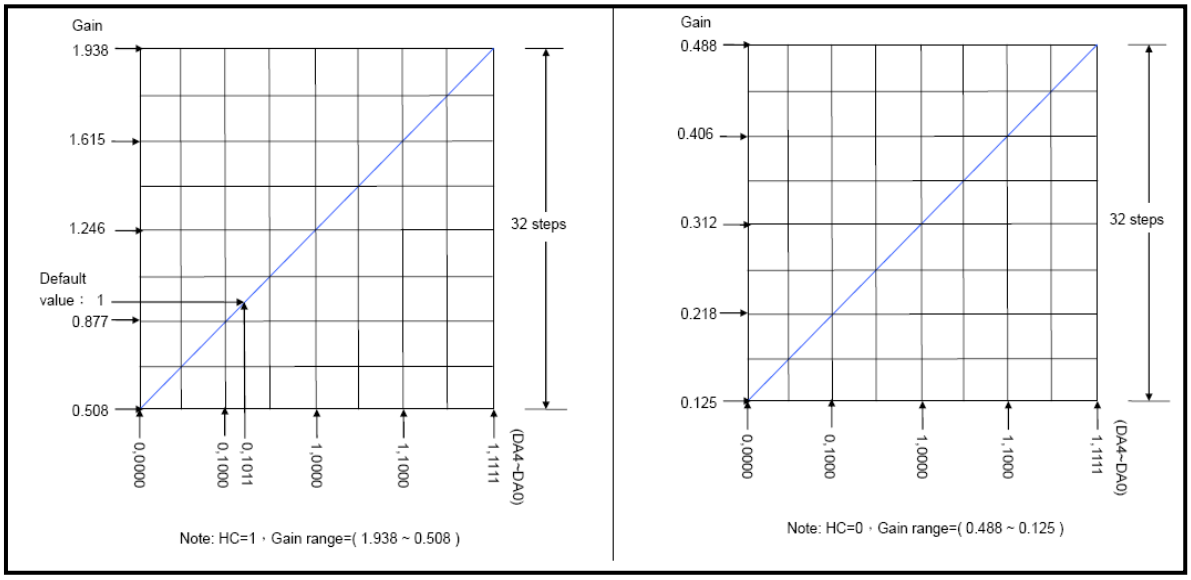

Figure 10. The relationship of current gain and gain code

Figure 11 is the relationship of output current and gain data under V_{DD}=5.0V and R_{ext}=1400Ω. The defaulted current gain, G =1, is corresponding to 10mA.

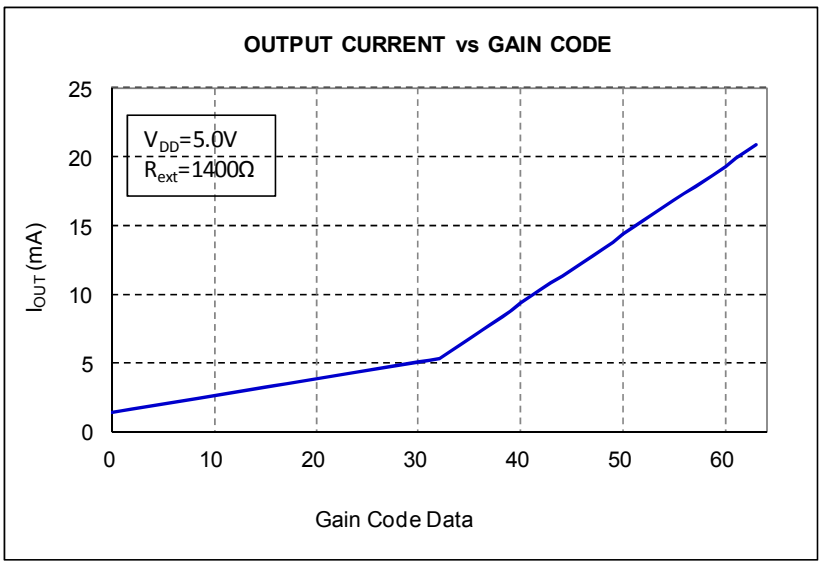

Figure 11. The relationship of output current and gain code at 5.0V, Rext=1400Ω.

Section 8: The Notice of LED Open-Circuit Error Detection

As figure 12 shows, MBI5152 executes the compulsory open-circuit detection while the LE high pulse is sampled by 7-DCLK rising edges. In the duration of compulsory open circuit detection, all the output channels will be turned off.

When LE high pulse pin is sampled by 1-DCLK rising edge, the result of open circuit detection will be shifted out from the SDO pin and the sequence is from MSB to LSB. The error detection will stop while the result is shifted out.

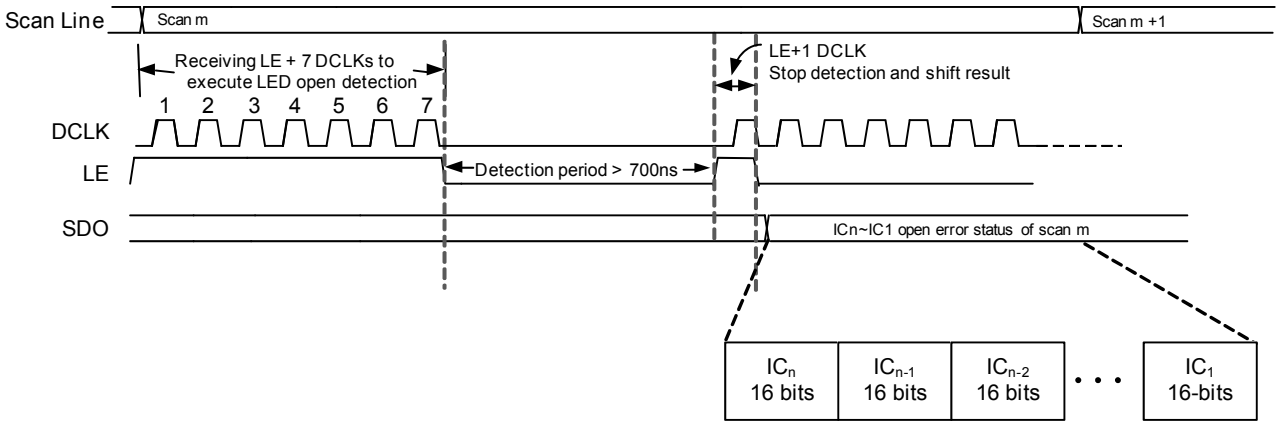

Figure 12. The timing diagram of compulsory open-circuit detection

In the duration of compulsory open-circuit detection, the SDI data can be ignored. In addition, the following notices must be taken

1. During the detection, the frame cannot display normal until LE arrested 1-DCLK rising edge. The duration should be keep longer than 700ns, as figure 12 shows.
2. When output turns on, please make sure the output voltage (V_{DS}) is higher than 0.3V. The bit [9:8] in configuration register 2 can choose open-circuit detection voltage by 0.3V/0.4V/0.5V/0.6V.
3. In the duration of compulsory open circuit detection, the scan line can't switch.
4. MBI5152 doesn't support LED short circuit detection.

Table 7. Error code

Status	Detected Result
Open	0
Normal	1

Section 9: Ghost Elimination in the Time-Multiplexing LED Displays

There are two types of ghosting problems in time-multiplexing application

1. The phenomenon of unexpected LED in last scan line slightly turns on called “upper ghost problem”. Please refer the follow method to prevent it.

   Figure 13 is an example of time-multiplexing application with n-scan lines. To avoid the upper ghost problem, the discharged circuit between the V_{LED} and GND of each scan line is recommended. Typically, the discharged circuit is a resistor cascaded with a zener diode. The resistance is about 390Ω~1kΩ, and the zener diode is about 3.0~3.3V, it can be adjusted based on the actual condition.

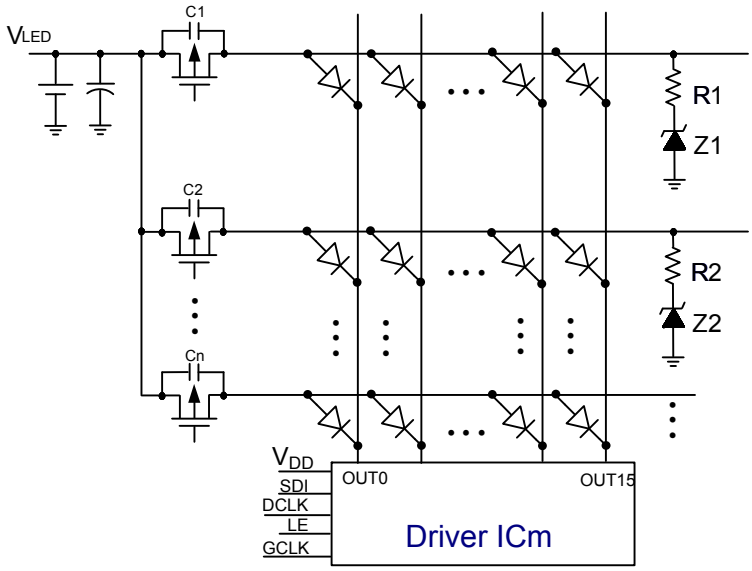

Figure 13. Circuit diagram of upper ghost elimination

2. The phenomenon of unexpected LED in next scan line slightly turns on called “lower ghost problem”.

   The bit[F] of configuration register1 is used to enable the lower ghost elimination, and figure 14 shows the timing diagram. In the dead time, the duration between the falling edge of 1025th GCLK and scan line switched determines the running time of lower ghost elimination.

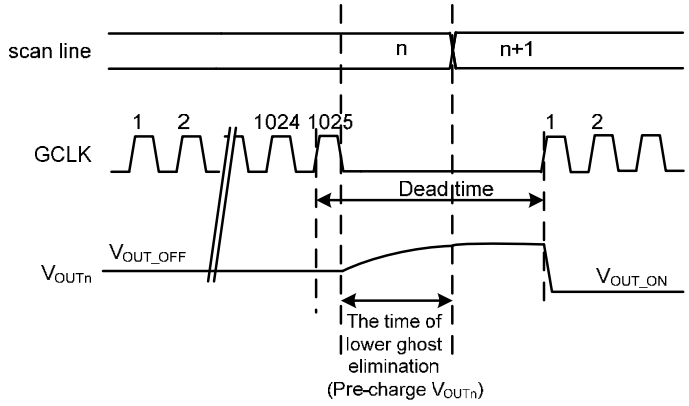

Figure 14. Timing diagram of lower ghost elimination

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Figure 15 shows the display example with diagonal line pattern, the ghost problem is apparent, and figure 16 shows the improvement which has enabled the lower ghost elimination.

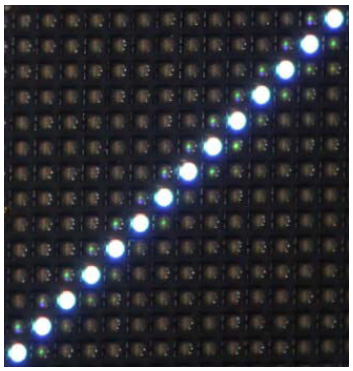

Figure 15. Display board with ghost problem

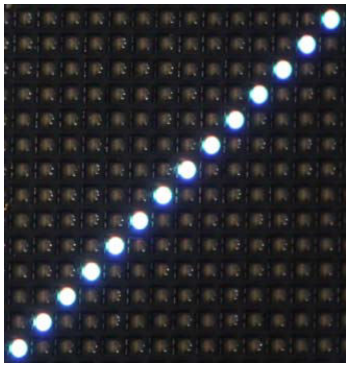

Figure 16. The display board with ghost elimination function

Enhance Mode of Lower Ghost Elimination

Not only enable lower ghost elimination can improve the lower ghost phenomenon, MBI5152 also provides enhance mode to eliminate the lower ghost phenomenon. De-ghost function must be enabled first, and then set the enhance mode according to the different loading, as table 8 shows.

Table 8. The setting table of enhance mode to eliminate the lower ghost

Configuration register 1 bit[F]	Configuration register 2 bit[D,C]	Comment
1	00、01(default)	Suitable for Red LED
1	10	Suitable for Green LED
1	11	Suitable for Blue LED

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Section 10: Improve the Dim Line Problem

In the time-multiplexing application, the parasitic capacitance exists in PCB layout trace, and is inconsistent in display board. The dim line problem is the most common problem in LED display, as figure 17 shows.

To improve this problem, the bit[3:1] in configuration register 2 is used to extend the output on-time. Figure 18 shows the improvement.

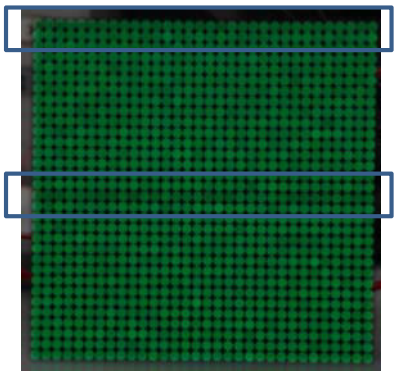

Figure 17. In 1:16 time multiplexing application, Green LED has dim line problem.

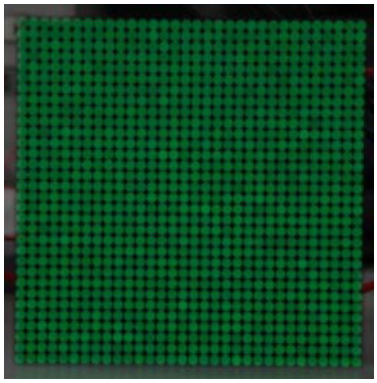

Figure 18. The Green LED dim line problem has been improved as configuration register 2 bit[3:1] set [100]: 18ns.

To extend the output on-time, there is one thing must be taken, the extended time can't longer than 1/2 of GCLK period, otherwise, the extend function will be invalid. For example, if the GCLK frequency is 20MHz, and the period time of GCLK (T_{GCLK}) is 50ns, then the extended output on-time can't longer than 25ns.

Section 11: Software Reset

When the software reset command is enabled, the internal counters of GCLK and data latch will be reset, and turned off all the output channels. However, the gray scale data stored in the SRAM, configuration register and current gain won't be reset.

Summary

MBI5152 uses the embedded S-PWM to control LED current and provides a storage solution of 8K-bit SRAM. Users don't need to send new data every time. This article provides the design guideline for uses.

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